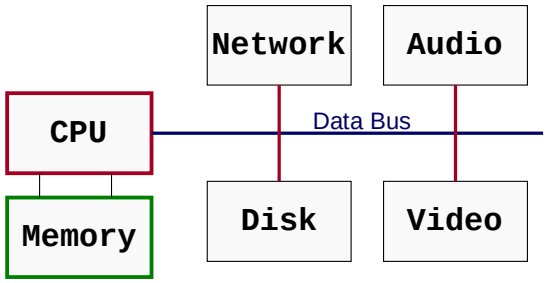
Building Computers from Digital Circuits

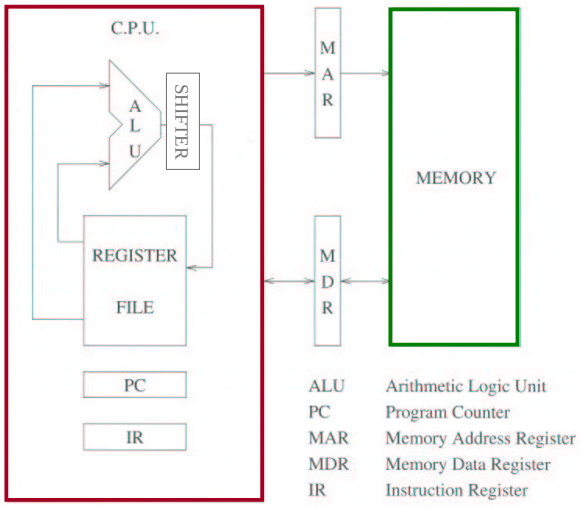
CS 217

Computer Architecture

- Simplified computer architecture



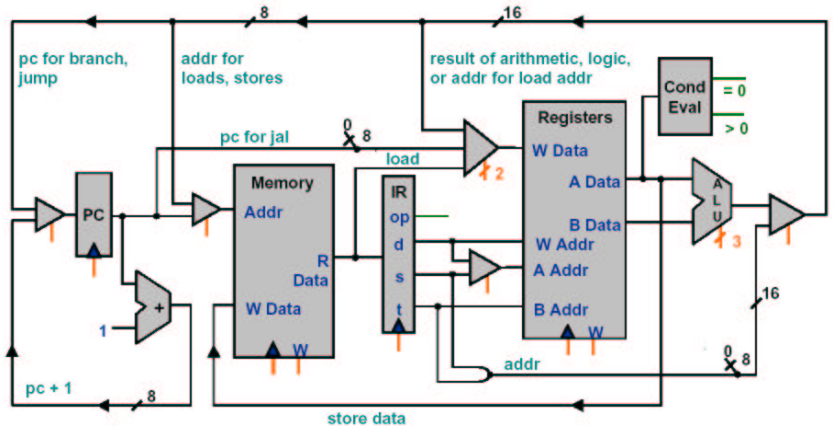
SPARC Architecture



ALU	Arithmetic Logic Unit
PC	Program Counter
MAR	Memory Address Register
MDR	Memory Data Register
IR	Instruction Register

Paul Fig 1.5 3

Toy Architecture (from CS126)



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Circuit components


AND gate x & y


OR gate x | y


NOT gate ~x

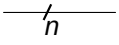
D Flipflop


Wire


Wires crossing

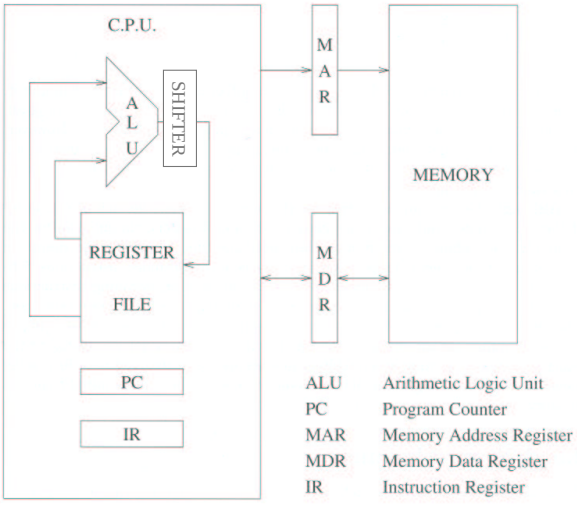

Wire connection

How do you build a computer out of these components?



n wires in parallel

SPARC Architecture



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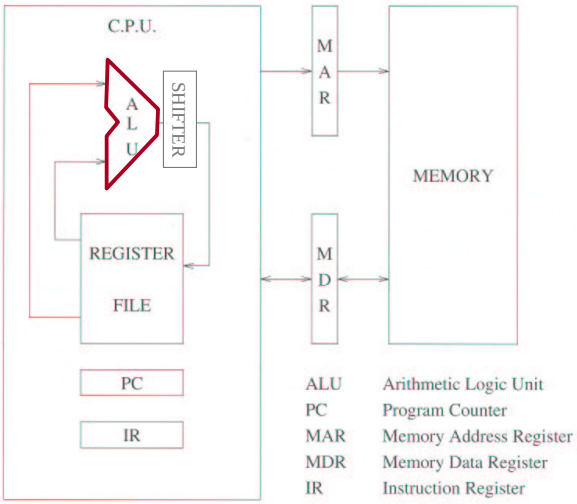
Paul Fig 1.5

SPARC Architecture



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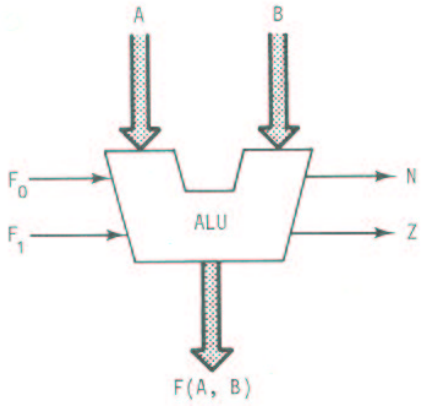
Arithmetic Logic Unit (ALU)

- Perform arithmetic operations
  - Boolean operations
  - Adding
  - etc.



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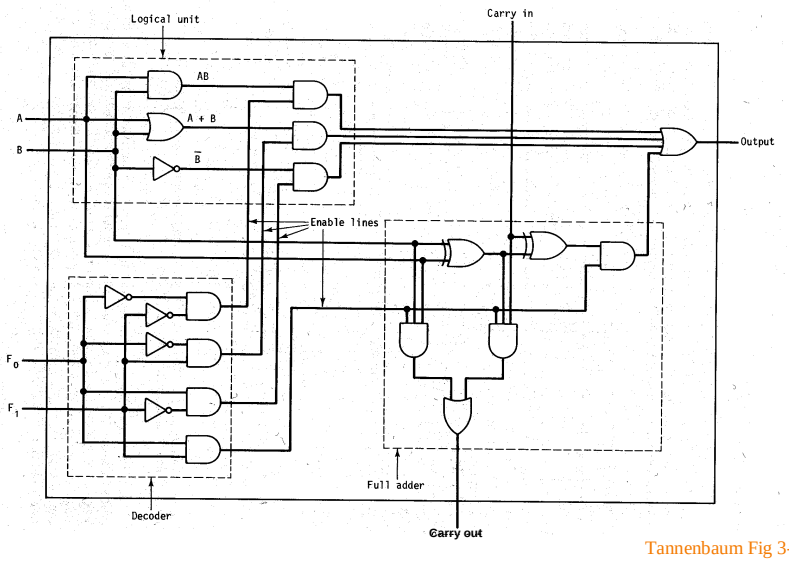
1-Bit Arithmetic Logic Unit



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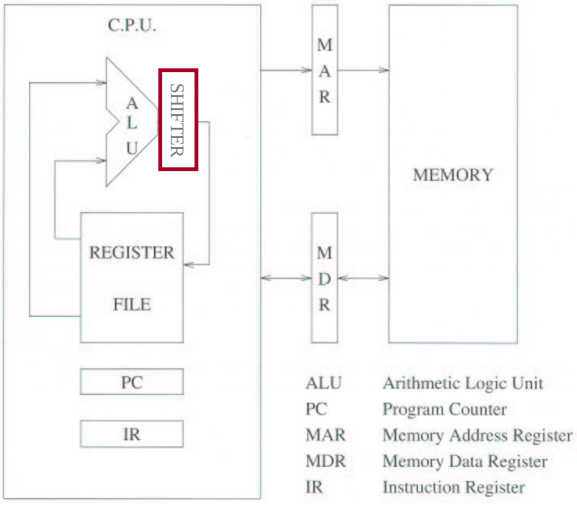
SPARC Architecture



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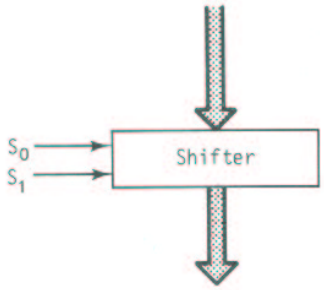
Shifter

- Shift bits to right or left



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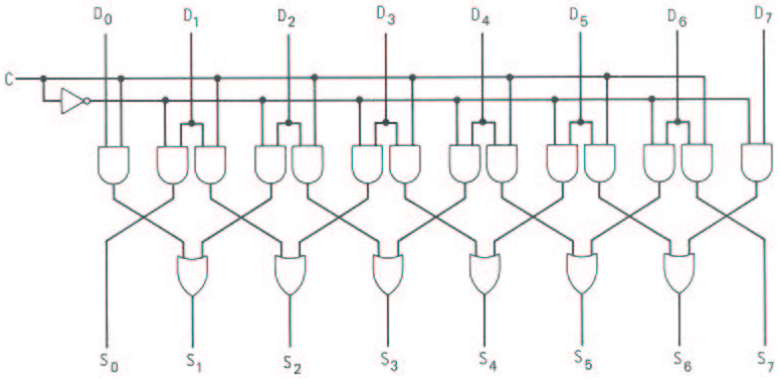
1-Bit Shifter

- Shift bits one spot to right or left



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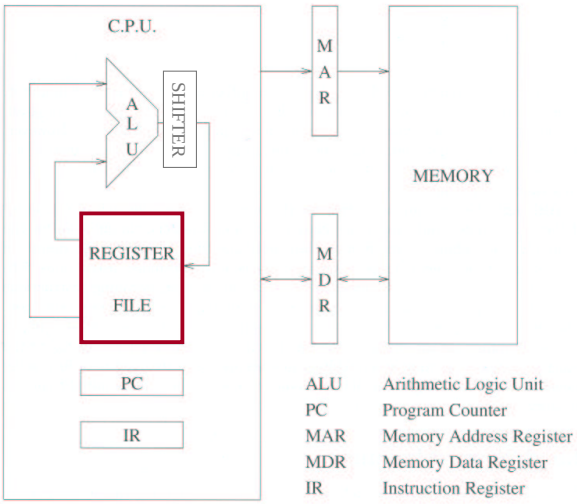
SPARC Architecture



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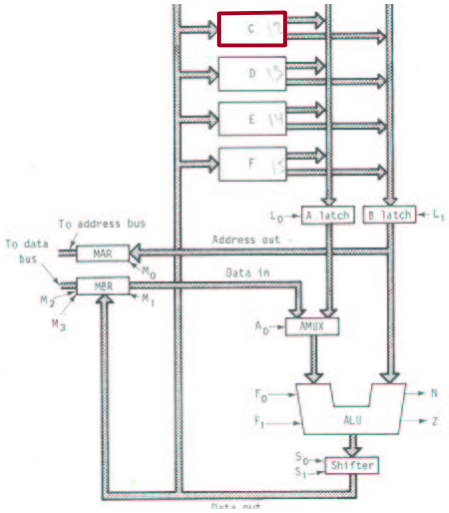
Register File

- Bank of registers connected to data buses



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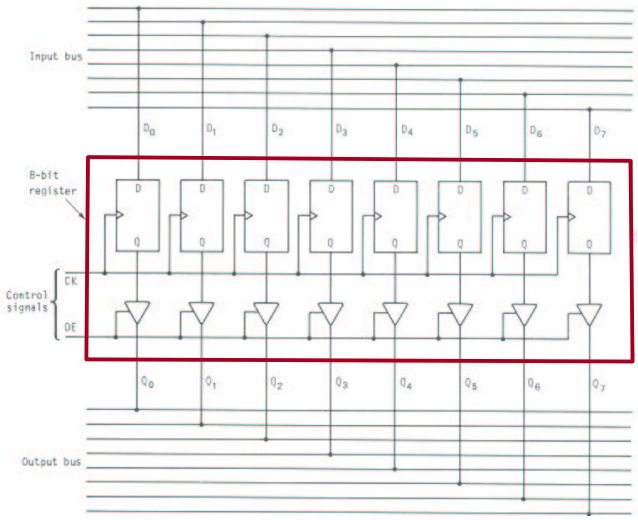
8-Bit Register



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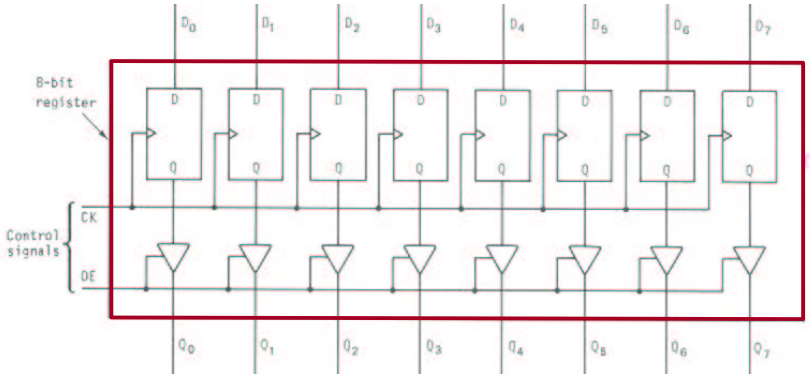
8-Bit Register



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Storage Hierarchy

- Registers
  - 32-128, 1-5ns access time (CPU cycle time)
- Cache
  - 1KB – 4MB, 20-100ns (multiple levels)
- Memory
  - 64MB – 2GB, 200ns
- Disk
  - 1GB – 100GB, 10ms
- Long-term Storage
  - 1TB, 1-10s

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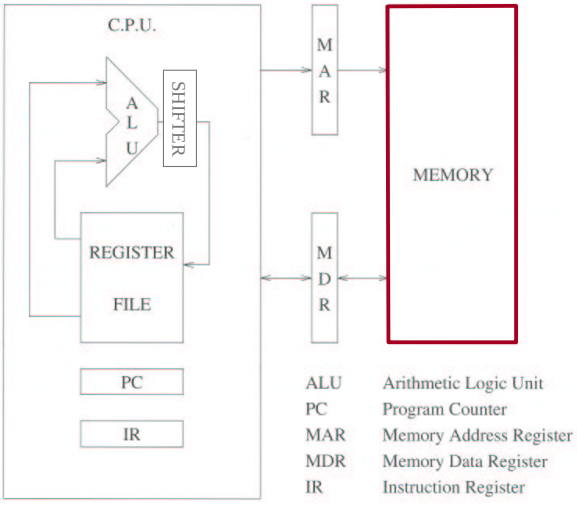
SPARC Architecture



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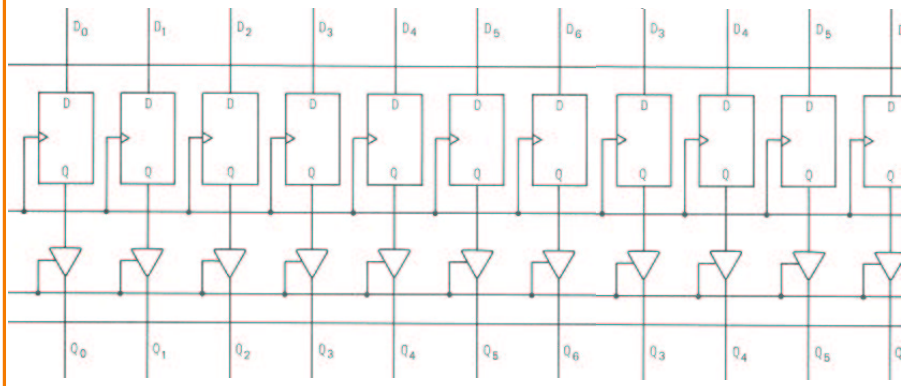
Memory

- Just string flip flops together?



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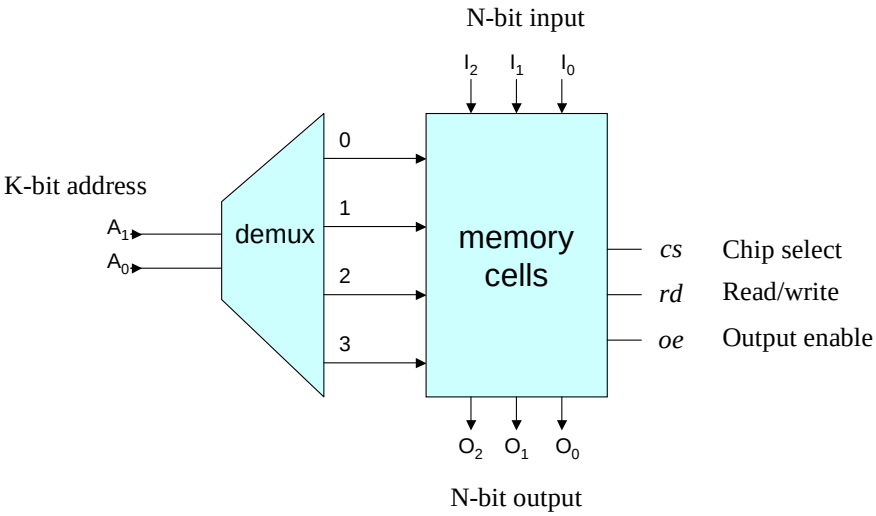
Addressable Memory



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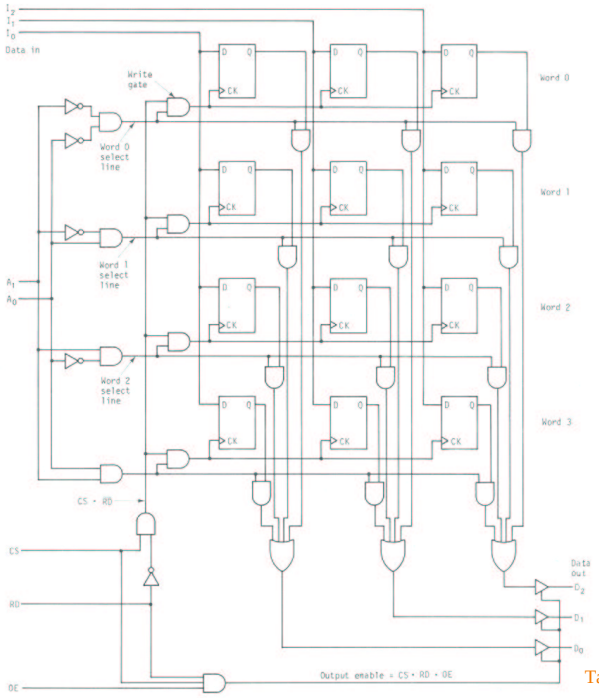
N-bit input

K-bit address

Chip select

Read/write

Output enable



N-bit output

Tannenbaum Fig 3-28

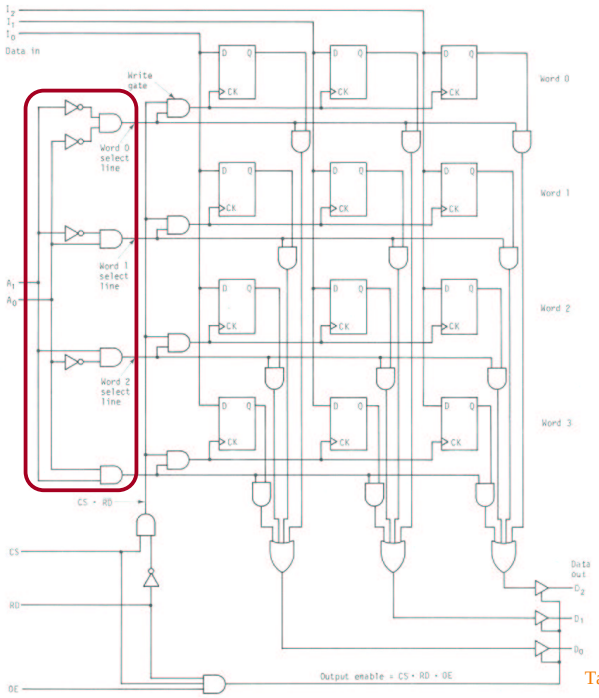
N-bit input

K-bit address

Chip select

Read/write

Output enable



N-bit output

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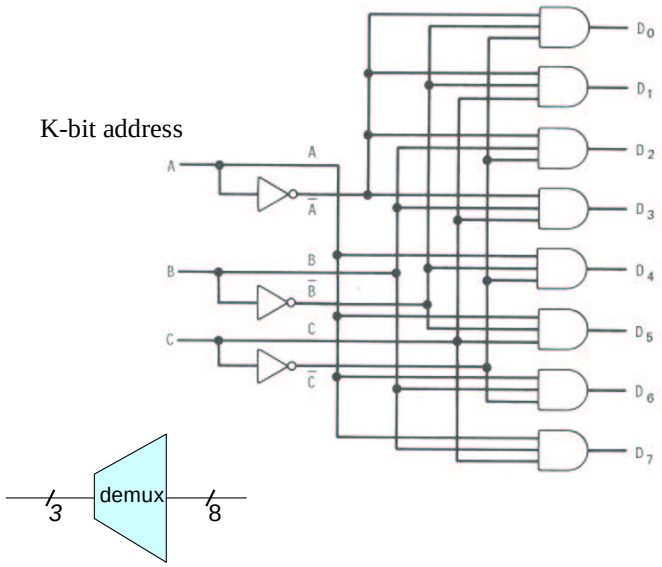
Demultiplexer



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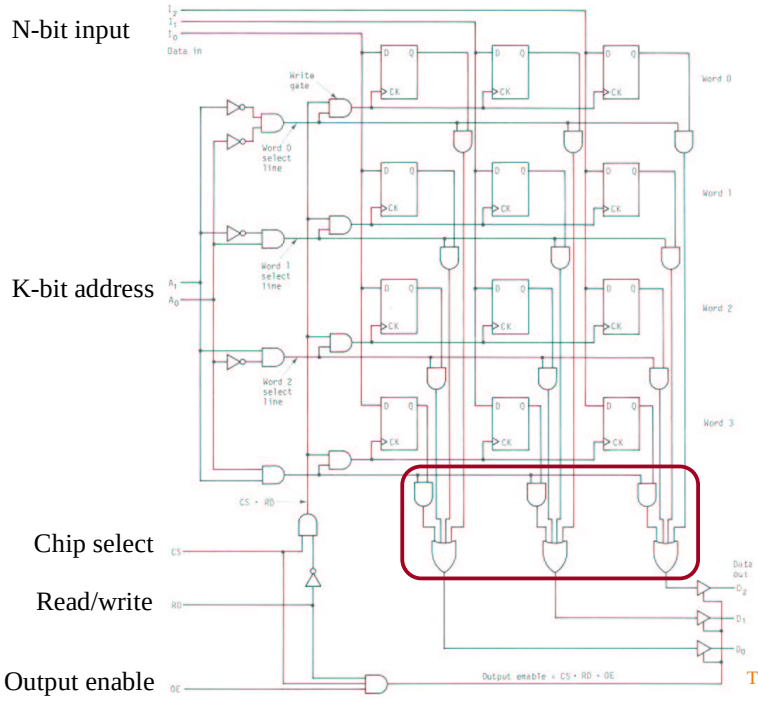

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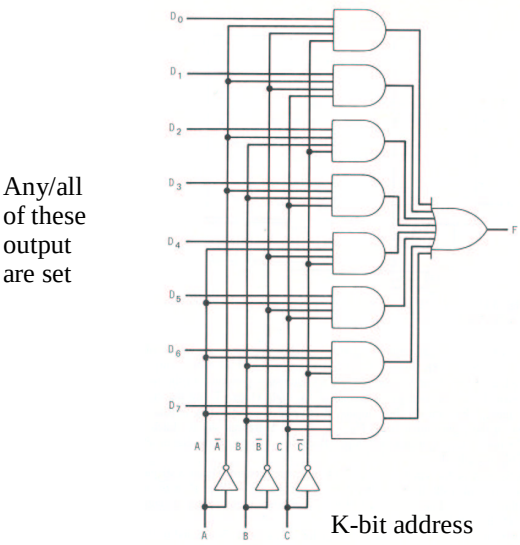
Multiplexer



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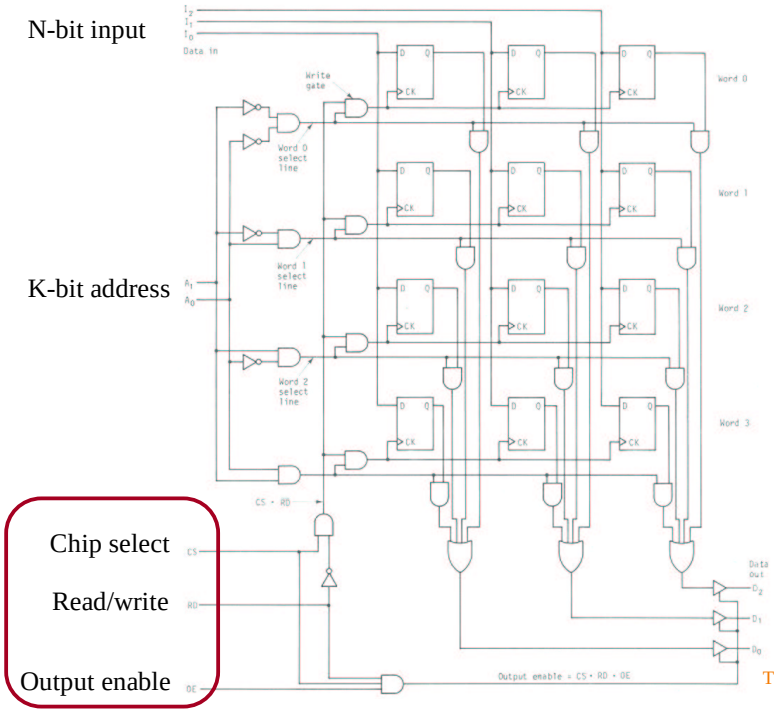

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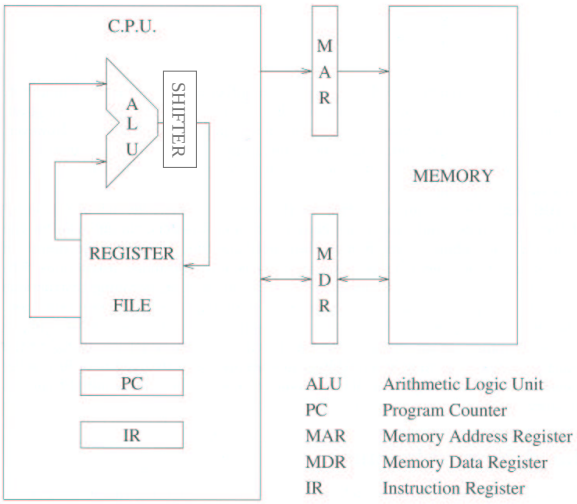
SPARC Architecture



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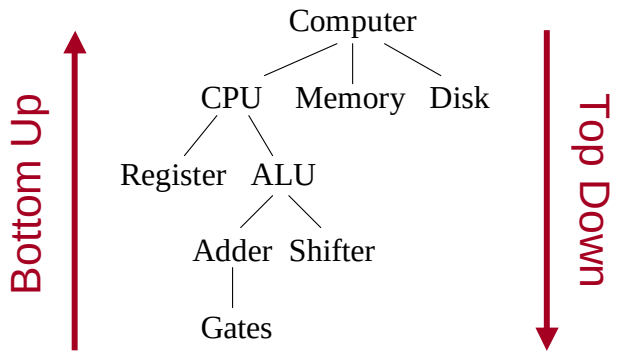
Design

- Possible strategies
  - Bottom-up
  - Top-down



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Summary

- Gates -> Computer
  - Components
  - Abstraction
  - Design
- Next time
  - Instruction set
  - Instruction processing

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