Topic 12: Register Allocation

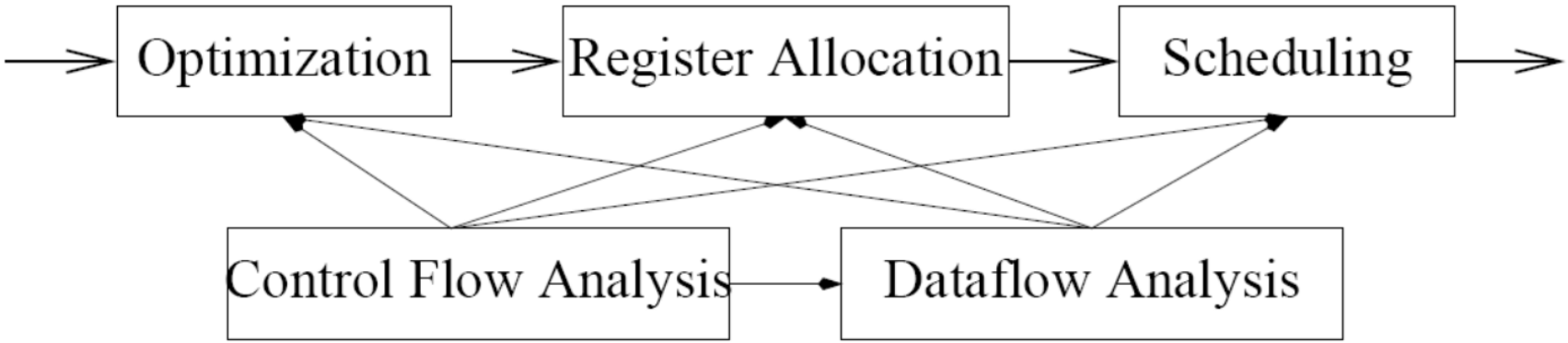
COS 320

Compiling Techniques

Princeton University
Spring 2016

Lennart Beringer

Structure of backend



Register allocation

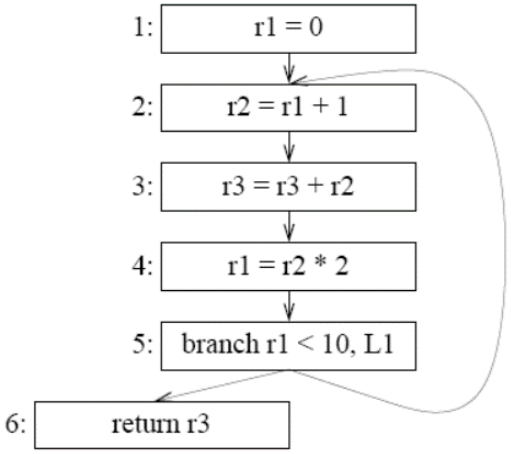
- assigns machine registers (finite supply!) to virtual registers
- based on liveness analysis: interference graph
- primary approach: graph coloring
- spilling
  - needed in case of insufficient supply of machine registers
  - idea: hold values in memory (stack frame)
  - transfer to/from registers to perform arithmetic ops, conditional branches, …
- architecture-specific requirements:
  - caller/callee-save
  - floating point vs integer, …

Recap: interference graph

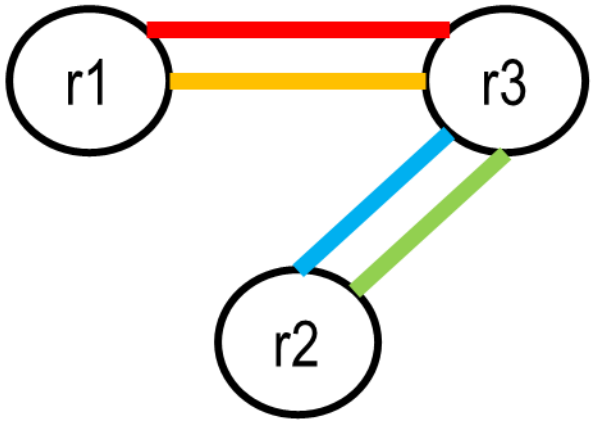
Liveness conflicts: virtual registers **x** and **y** **interfere** if there is a node **n** in the CFG such that **x** and **y** are both LiveOut at **n**.

Representation: conflict/interference graph:

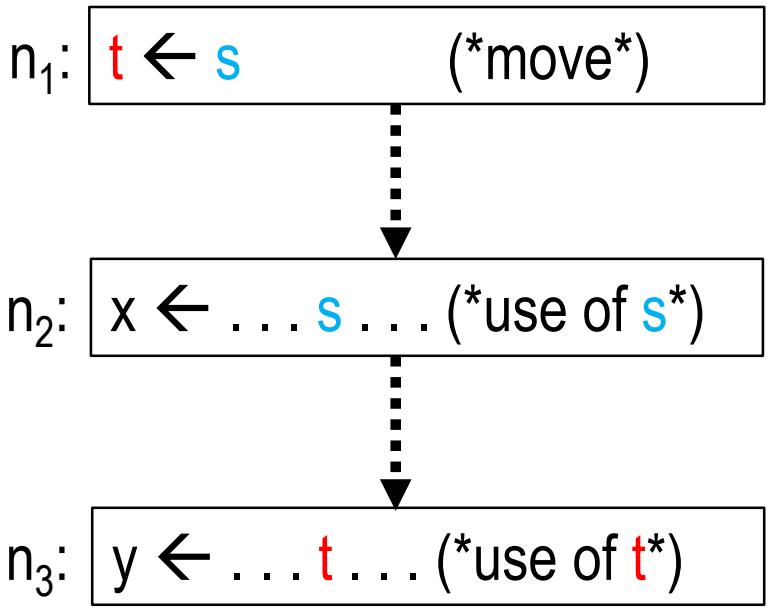
- each virtual register represented by one node
- Interference between **x** and **y**: undirected edge between nodes **x** and **y**



Node	*DEF*	OUT	IN
1	r1	r1,r3	r3
2	r2	r2,r3	r1,r3
3	r3	r2,r3	r2,r3
4	r1	r1,r3	r2,r3
5	-	r1, r3	r1,r3
6	-		r3



Interference graph: optimization for MOVEs



Virtual registers s and t

- are both live-out at n_1
- hence interfere formally

- will hence be assigned different registers

But: we'd like them to share a register, and to eliminate the move instruction!

Solution: treat move instructions differently during interference analysis

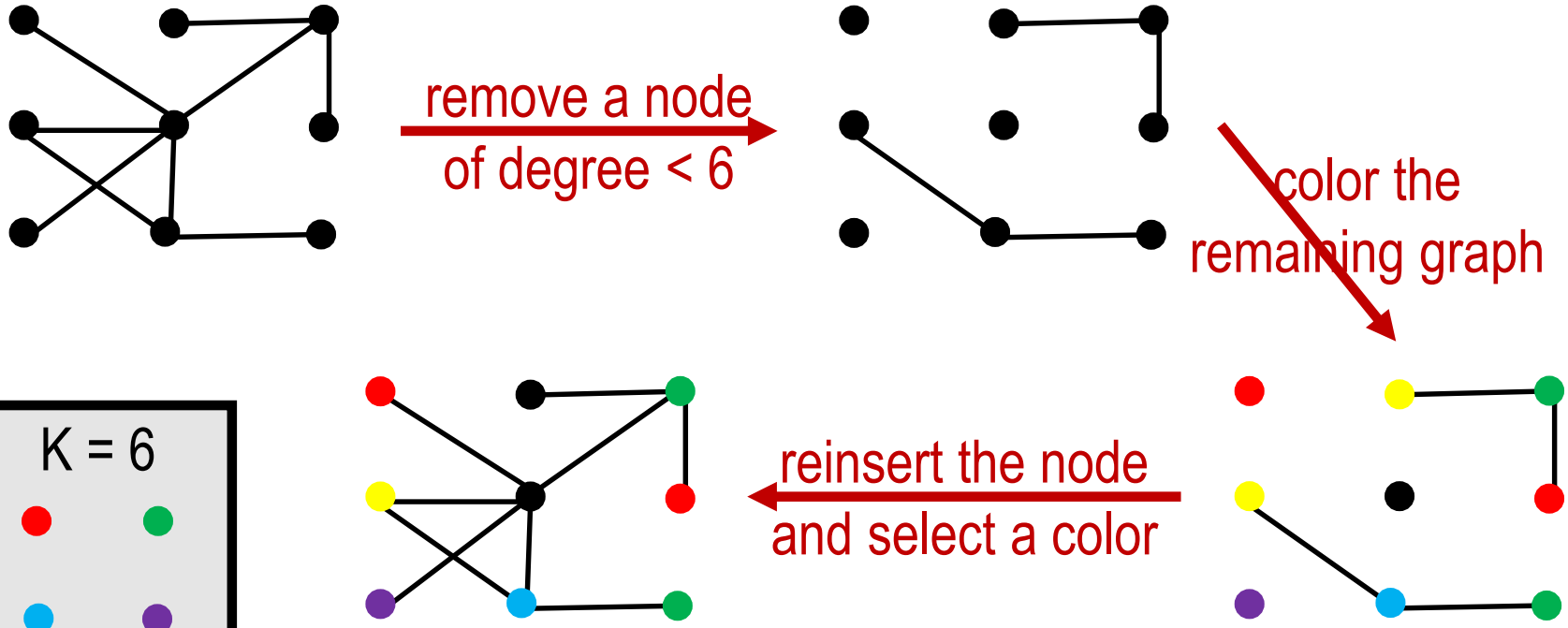
For n: a ← c (*move*) and liveOut(n) = $\{b_1, \ldots, b_k\}$, only add edges

for those b_i that are different from c.

Graph coloring using Kempe's heuristics (1879)

Observation:

- suppose G has a node m with < K neighbors
- if G – {m} can be K-1 colored, G can be K-colored:
  - m's neighbors use at most K-1 colors in G - {m}
  - so can reinsert m into G and select a color

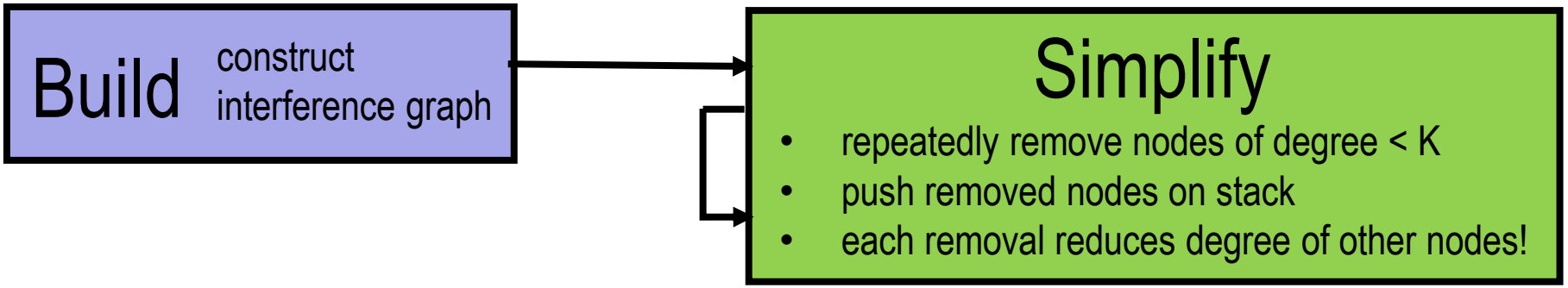


➔ recursive (stack-based) algorithm

Optimistic coloring using Kempe

Build construct interference graph

Optimistic coloring using Kempe



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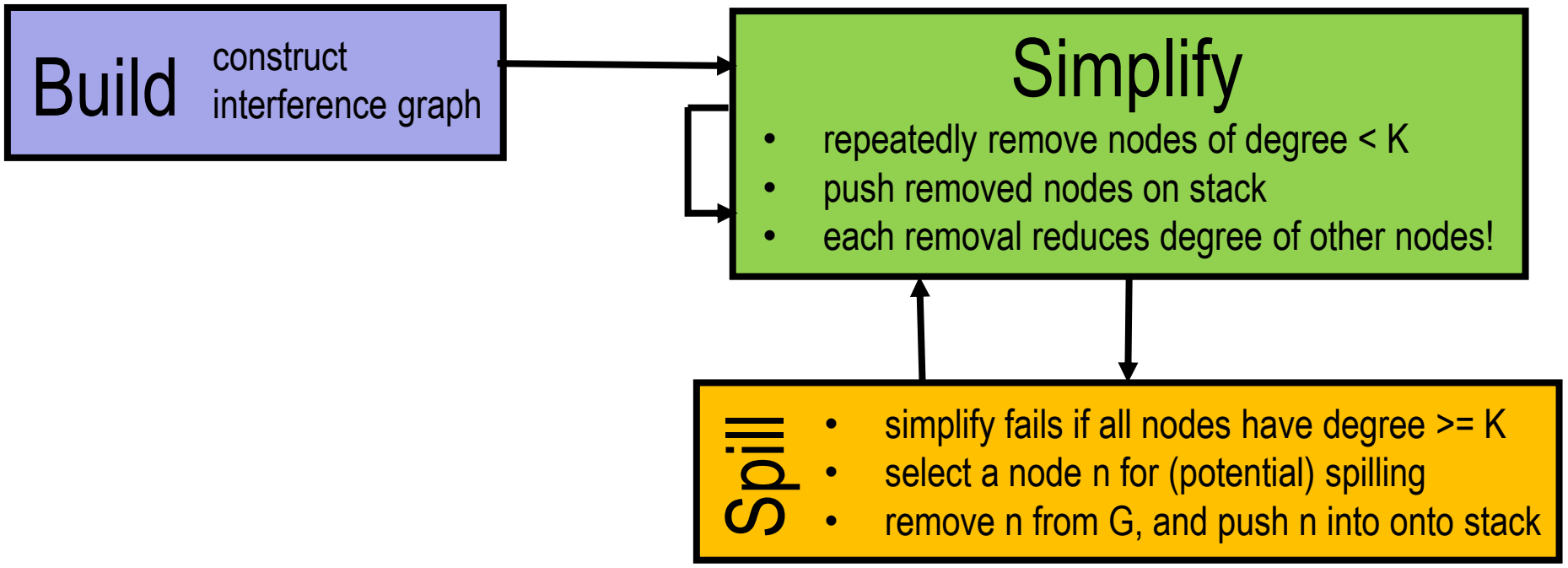

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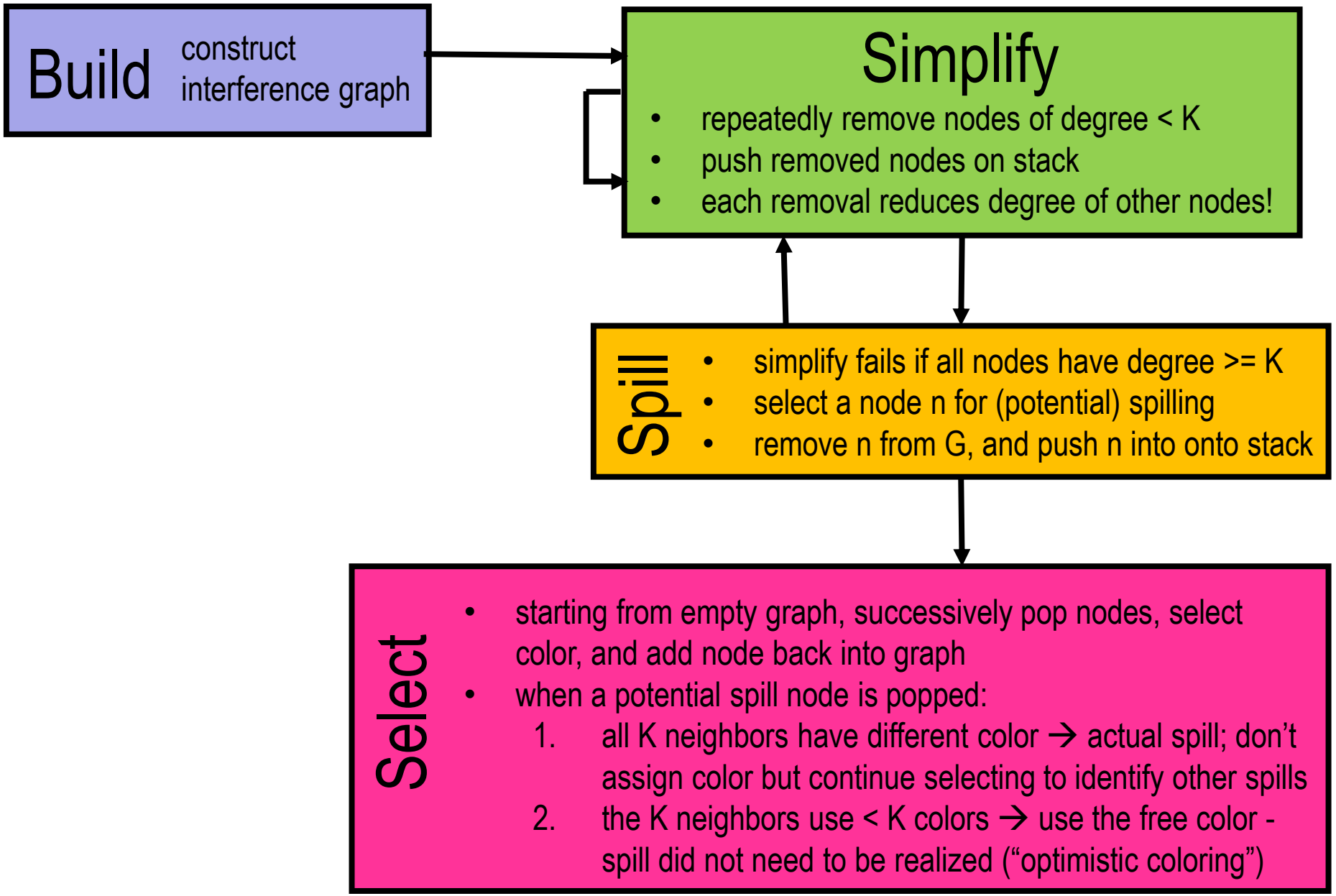

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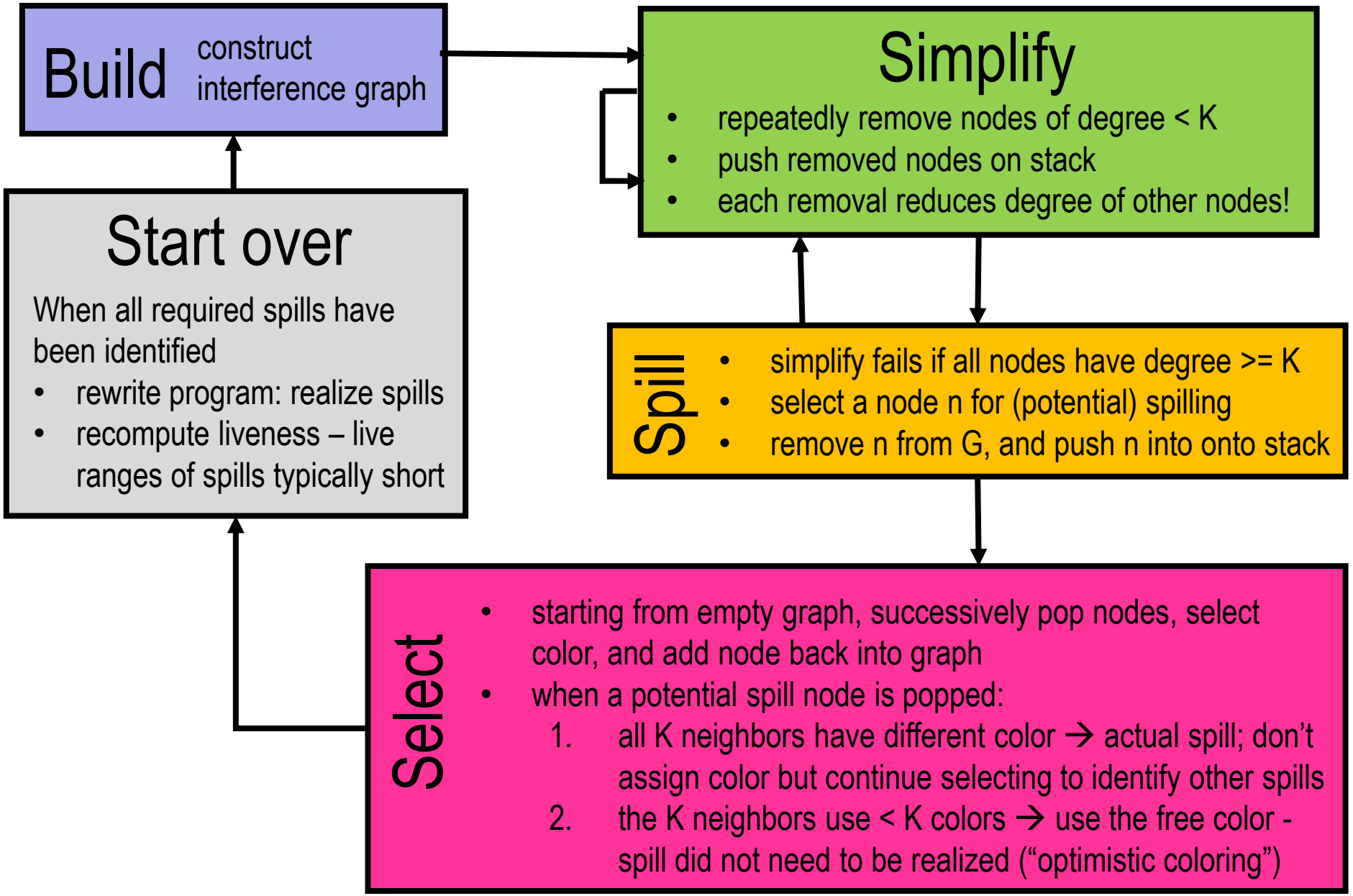
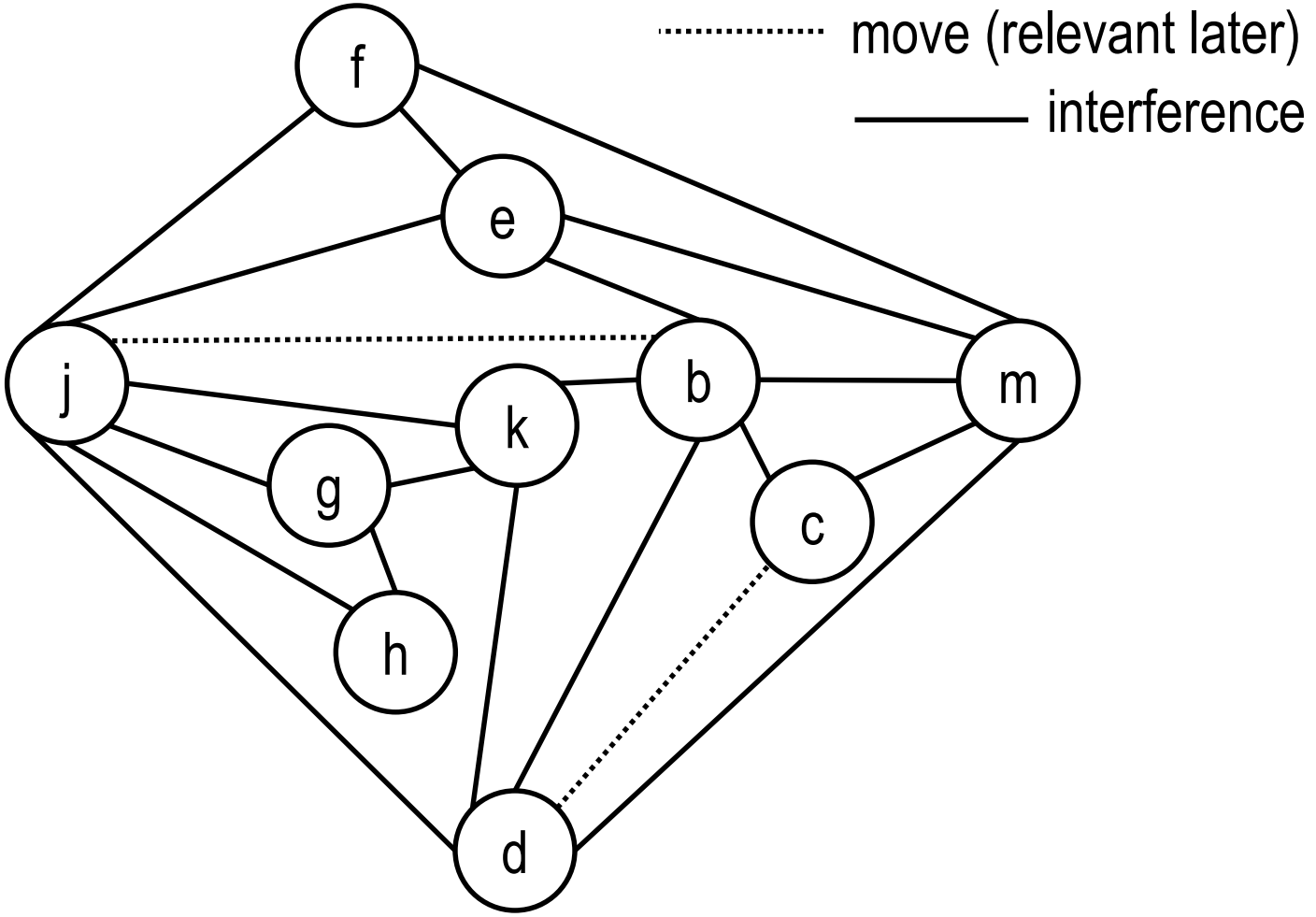


Basic coloring: example (K = 4)

```
// liveIn: k, j
g := M [ j+12 ]
h := k – 1
f = g * h
e := M [ j + 8 ]
m := M [ j + 16 ]
b := M [ f ]
c := e + 8
d := c
k := m + 4
j := b
// liveOut d k j
```



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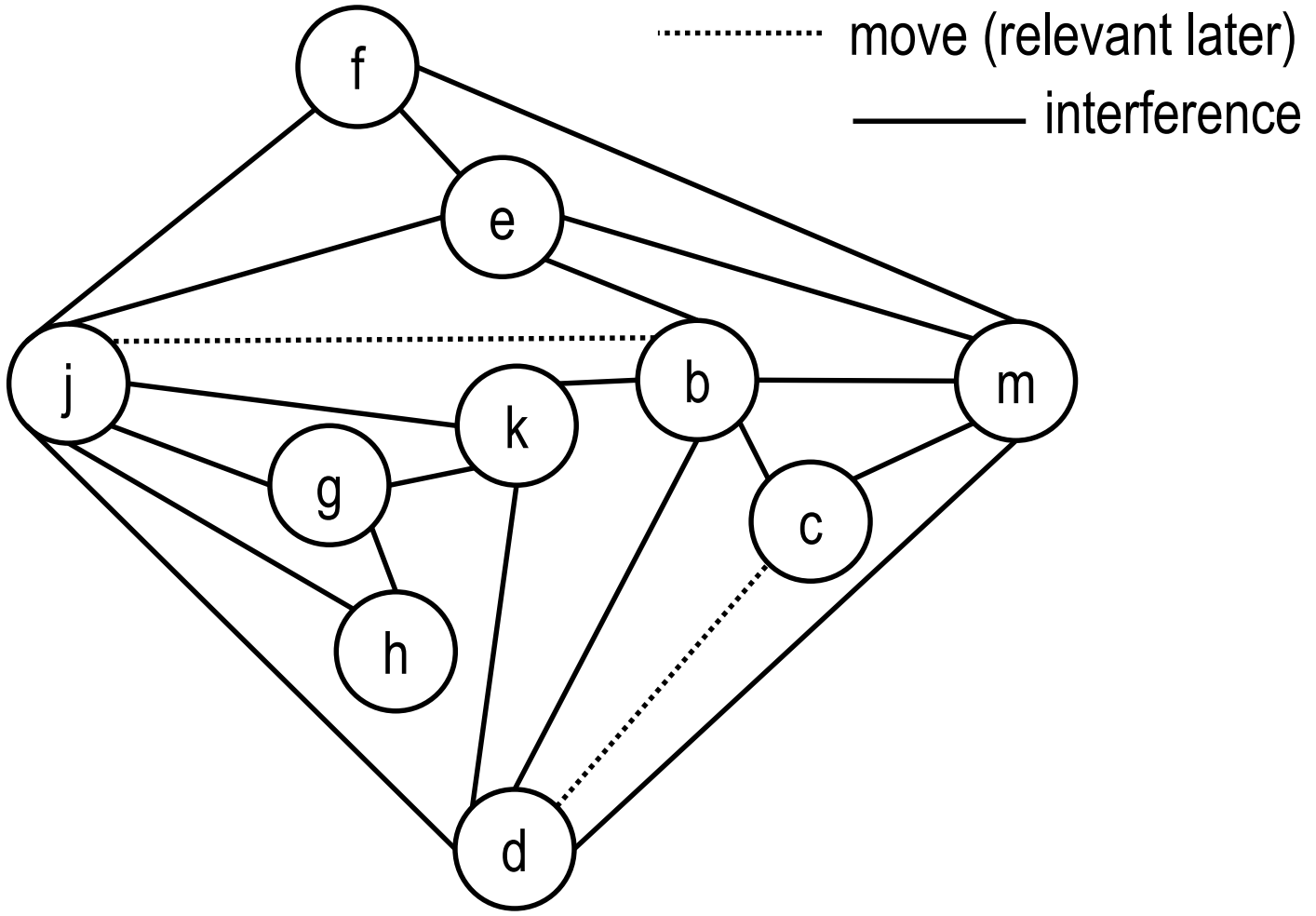

Nodes of degree < K: c, g, h, f

→ push g, h

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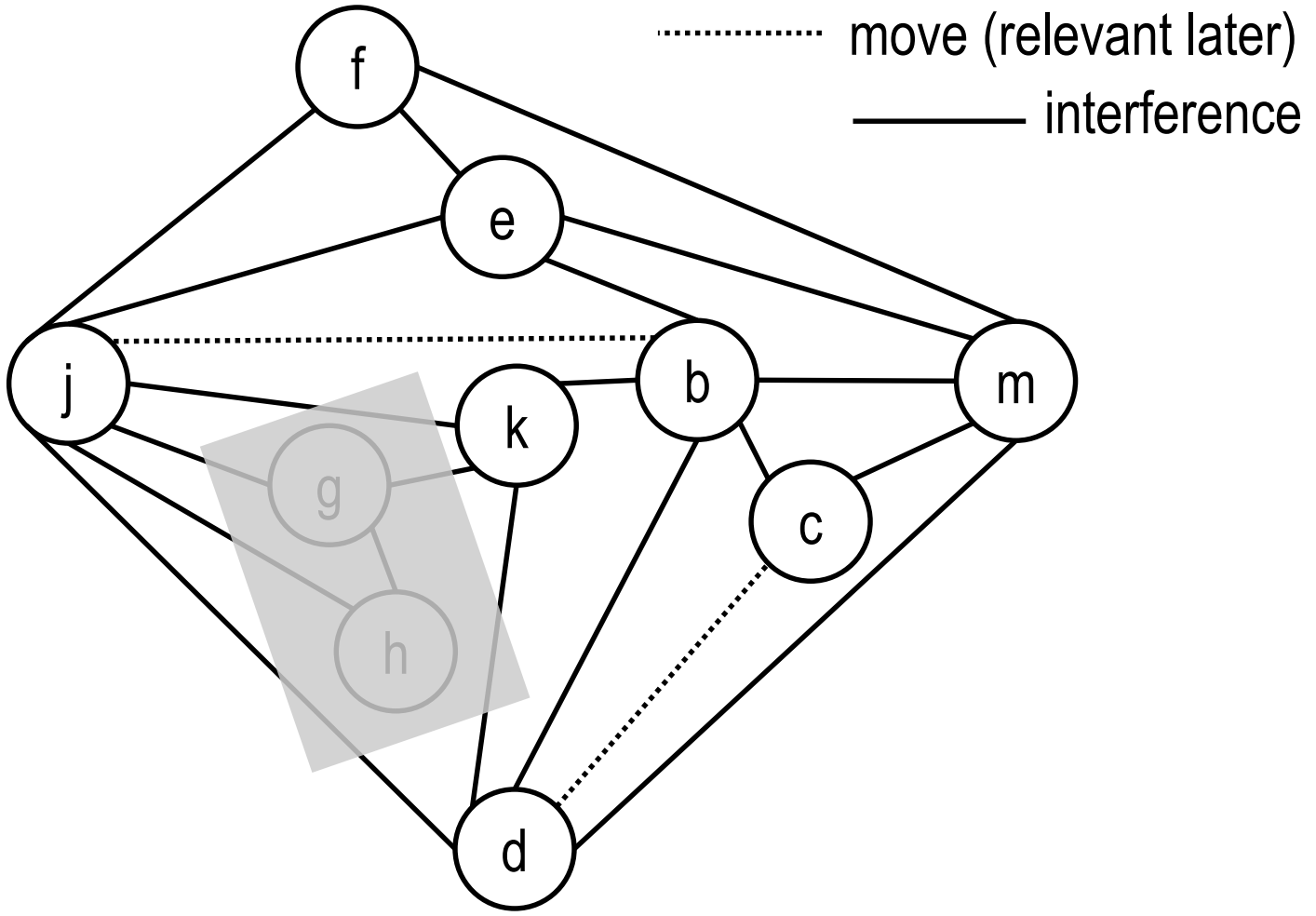

Nodes of degree < K: c, f

→ push g, h

Next: **push** k, d, j, e, f, b, c

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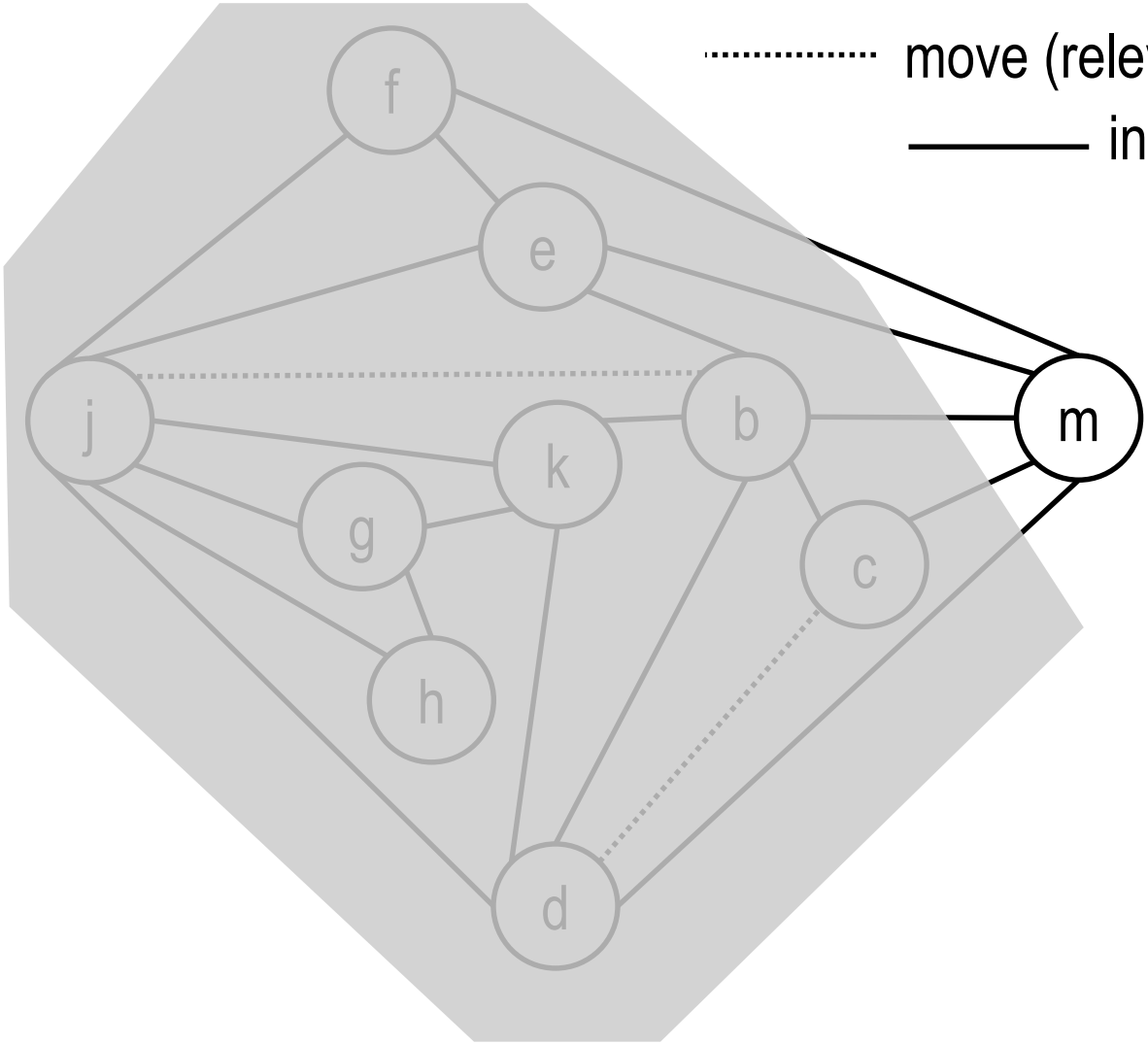

Nodes of degree < K: m

→ push g, h, k, d, j, e, f, b, c

Next: **push** m, **pop** m

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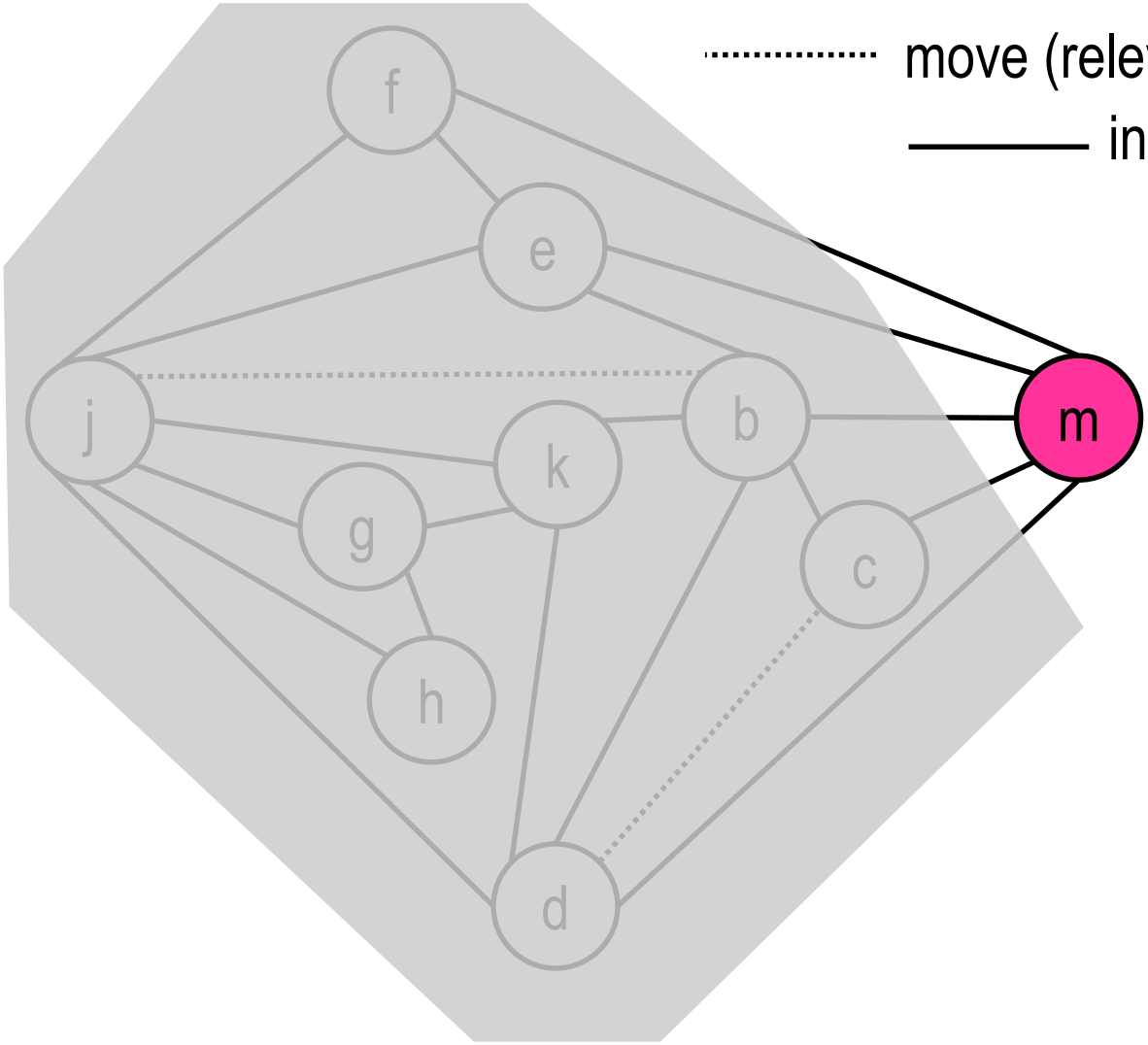

Nodes of degree < K:

→ push g, h, k, d, j, e, f, b, c

Next: **pop** c, b, f

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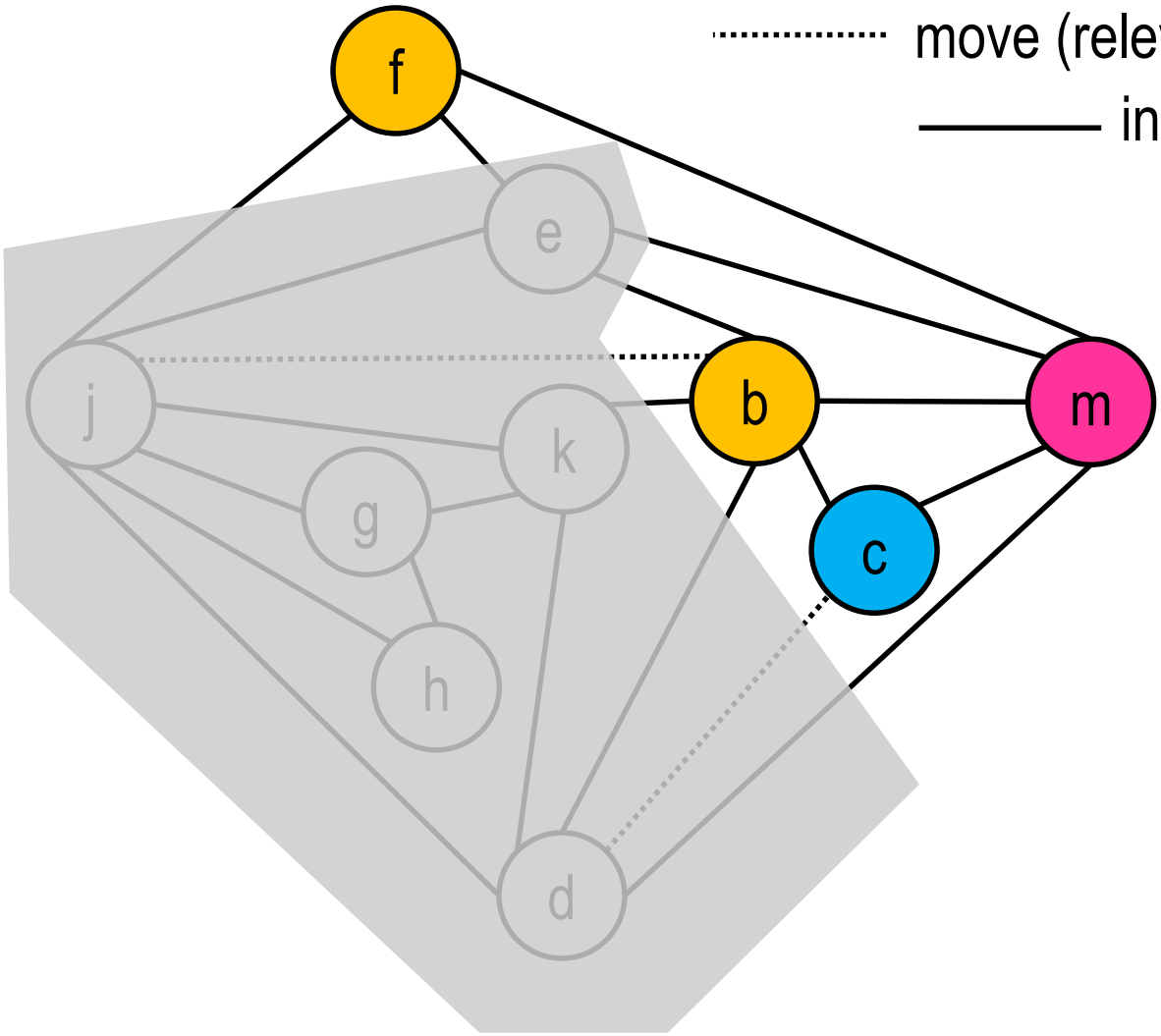

Nodes of degree < K:

→ push g, h, k, d, j, e

Next: **pop** e, j, d

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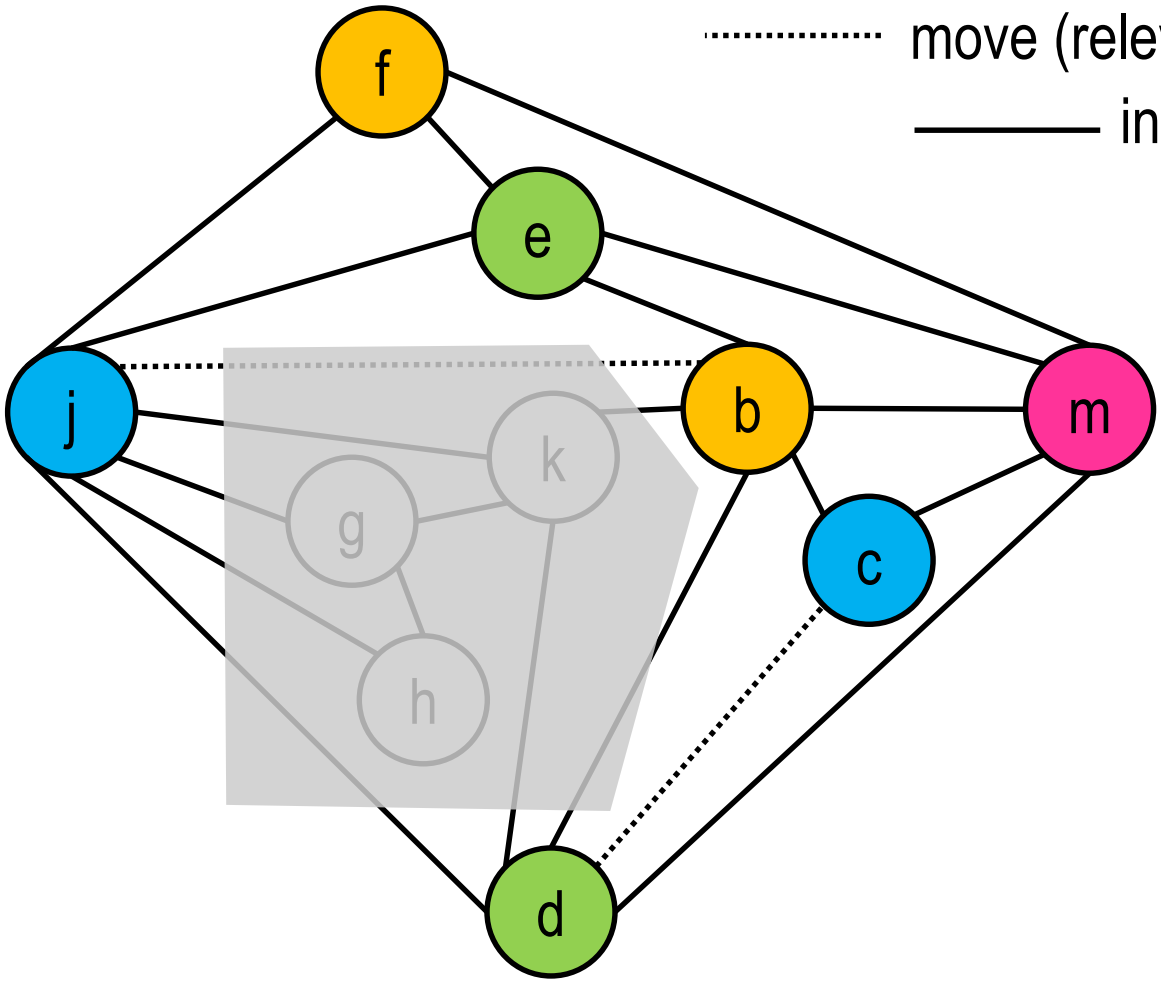

Nodes of degree < K:

→ push g, h, k

Next: **pop** k, h, g

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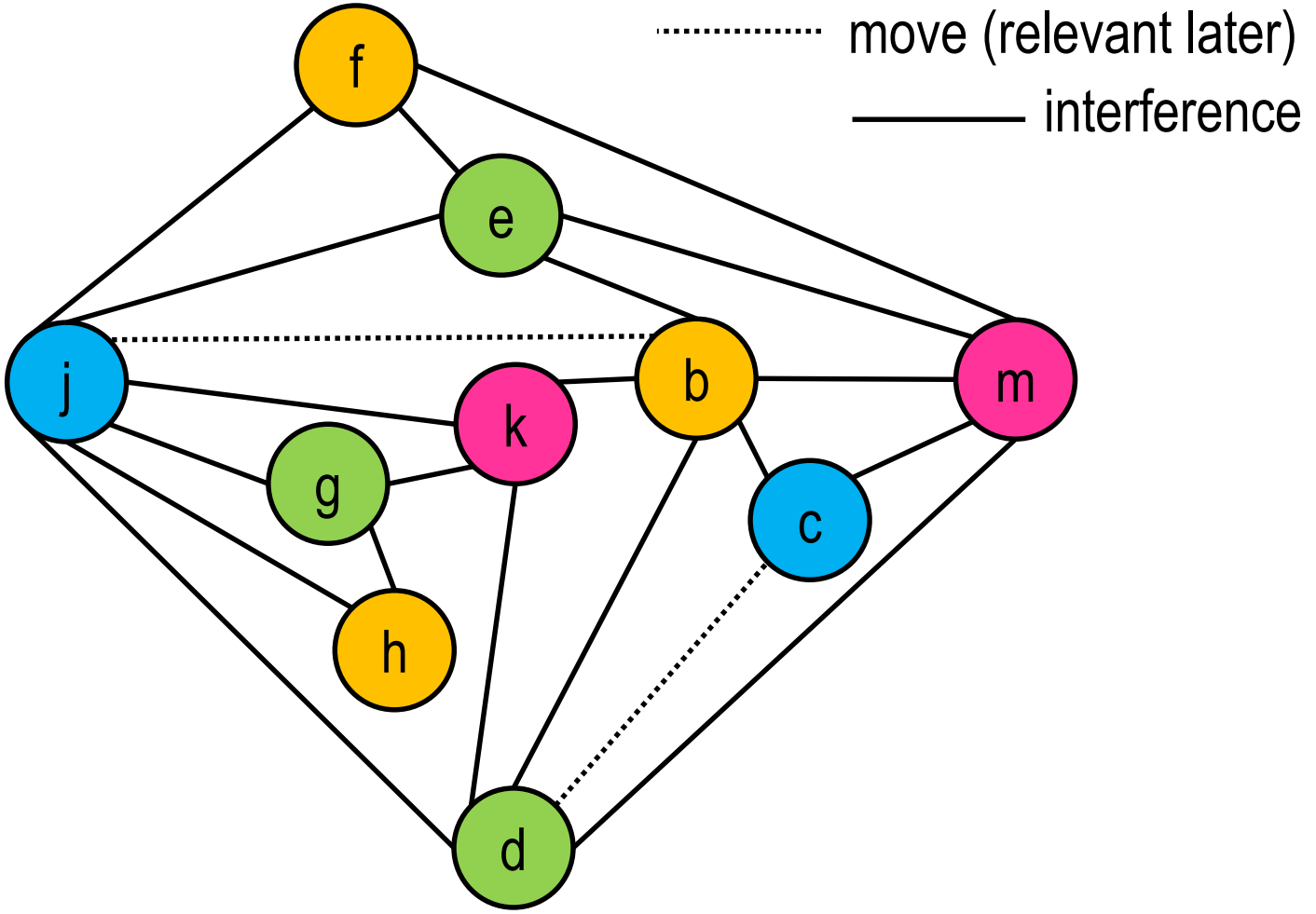


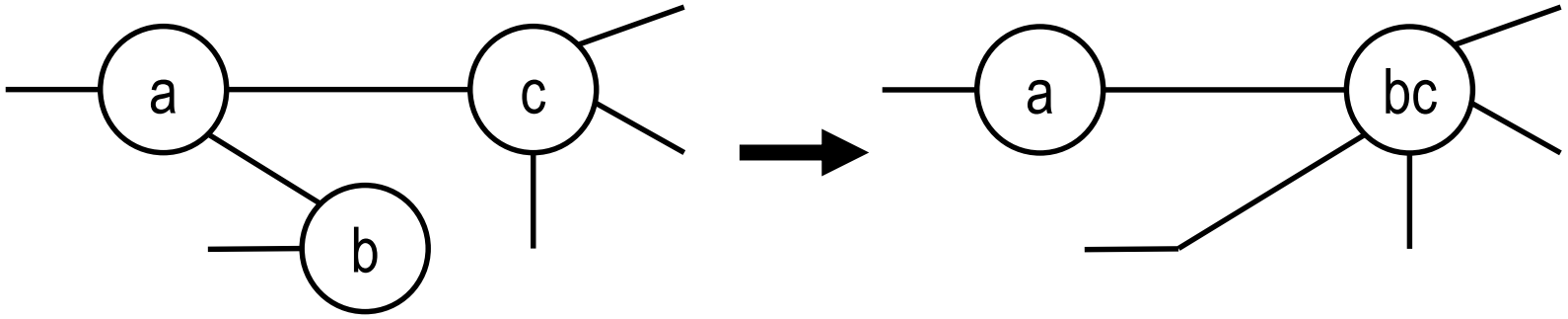
Nodes of degree < K:

→ Stack empty

Done – no spilling needed

Register coalescing

Nodes in the conflict graph can be coalesced, provided that they don't interfere; edges of coalesced node = union of edges associated with original nodes



In particular: if source and dest of a move don't interfere, coalescing allows one to eliminate the move instruction.

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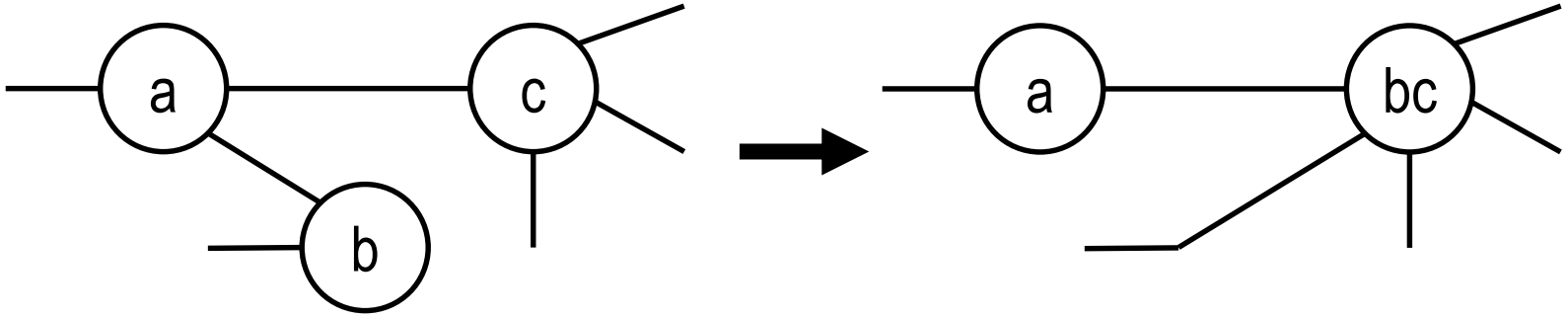
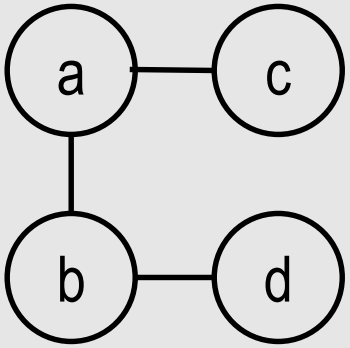


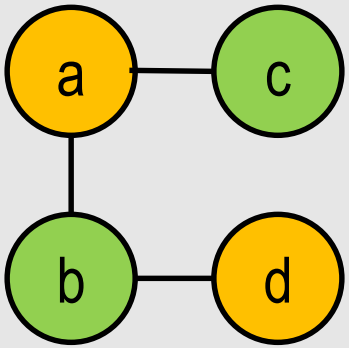
In particular: if source and dest of a move don't interfere, coalescing allows one to eliminate the move instruction.

But: coalescing before coloring may make graph not colorable!

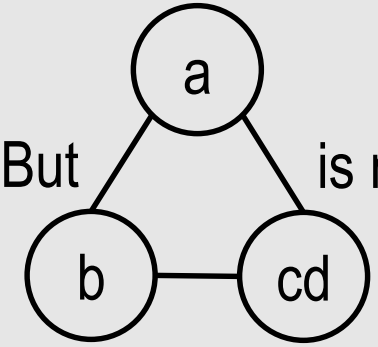
Example:



is 2-colorable:



. But



is not.

Safe coalescing heuristics: Briggs

Coalesce nodes that don't interfere, provided that the resulting merged node has less than K neighbors of degree ≥ K.

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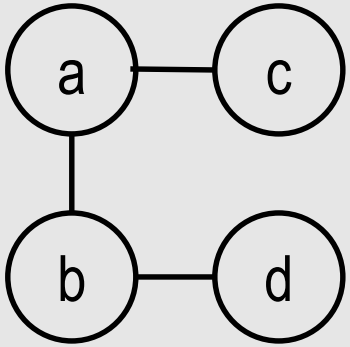
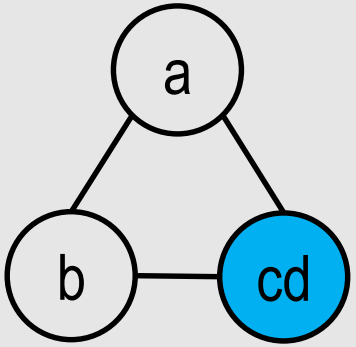


Don't merge c with d, since deg(a)=deg(b) = 2 in



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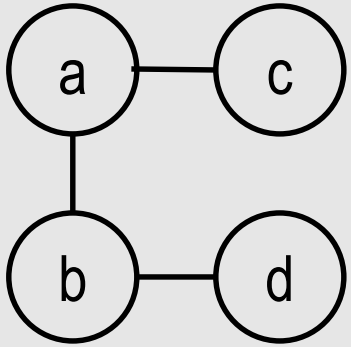

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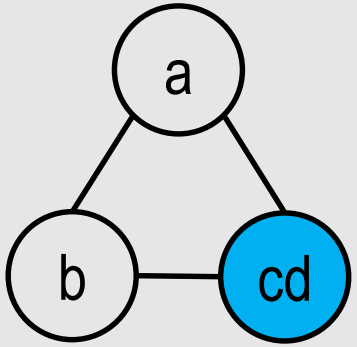

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Why is this safe?

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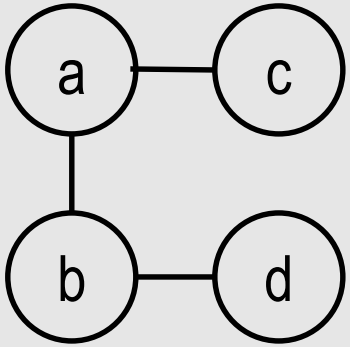

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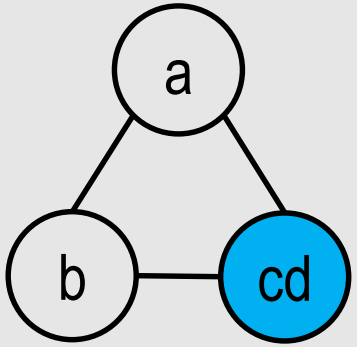

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- after simplification, all nodes of degree < K have been eliminated

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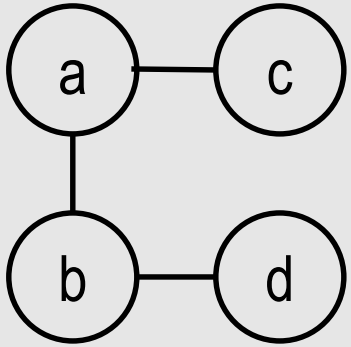

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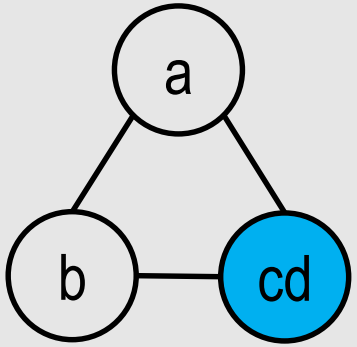

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- after simplification, all nodes of degree < K have been eliminated
- so only high-degree neighbors of merge remain

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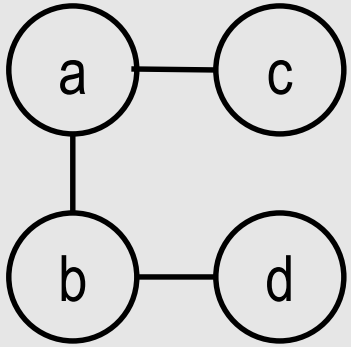

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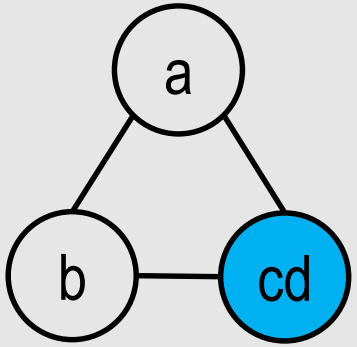

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Why is this safe?

- after simplification, all nodes of degree < K have been eliminated
- so only high-degree neighbors of merge remain
- if there are < K of such neighbors, the degree of the merge is < K, so we can simplify merge

Hence, merging does not render a colorable graph incolorable.

Safe coalescing heuristics: George

Coalesce noninterfering nodes x and y only if every neighbor t of x already interferes with y or is of degree < K.

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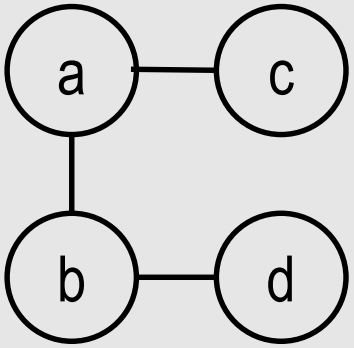

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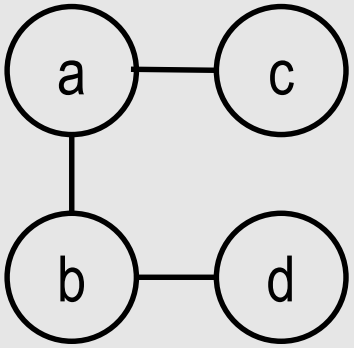

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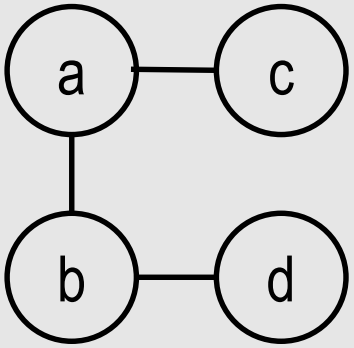

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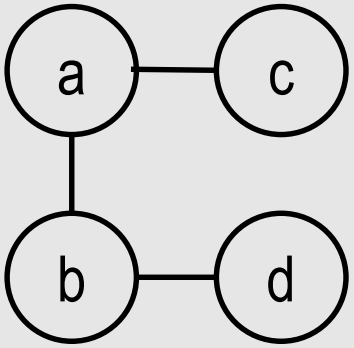

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- if coalescing is **not** performed, all nodes in S simplify, leaving a reduced graph G_1

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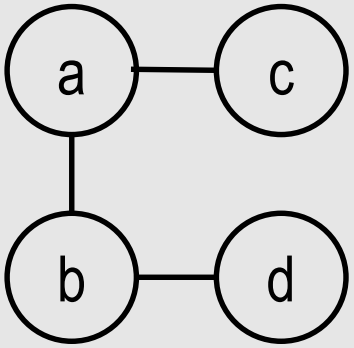

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- if coalescing is **not** performed, all nodes in S simplify, leaving a reduced graph G_1
- if coalescing **is** performed, simplify also removes all nodes in S: each s ϵ S is of degree < K or is already adjacent to both x and y in G, so still simplifies after merging of x and y

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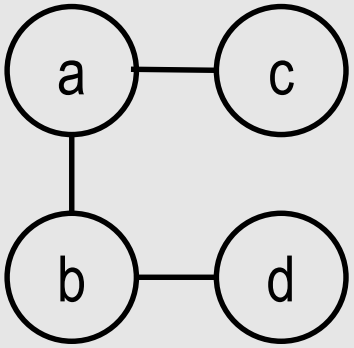

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- if coalescing is **not** performed, all nodes in S simplify, leaving a reduced graph G_1
- if coalescing **is** performed, simplify also removes all nodes in S: each s ϵ S is of degree < K or is already adjacent to both x and y in G, so still simplifies after merging of x and y
- the resulting G_2 is a subgraph of G_1 ("merge" in G_2 corresponds to y in G_1), so if G_1 can be colored, so can G_2

Again, merging does not render a colorable graph incolorable.

Safe coalescing heuristics: Briggs, George

Both heuristics are conservative:

- we may miss some opportunities to coalesce (HW: example?)
- specifically, we may fail to eliminate some move instructions
- but that's preferable to not coalescing at all, which results in more spills; spills significantly more expensive (time: load+store versus move; space)

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→ interleaving simplify with coalescing eliminates many moves, while still avoiding many spills. Thus, refine our allocation procedure:

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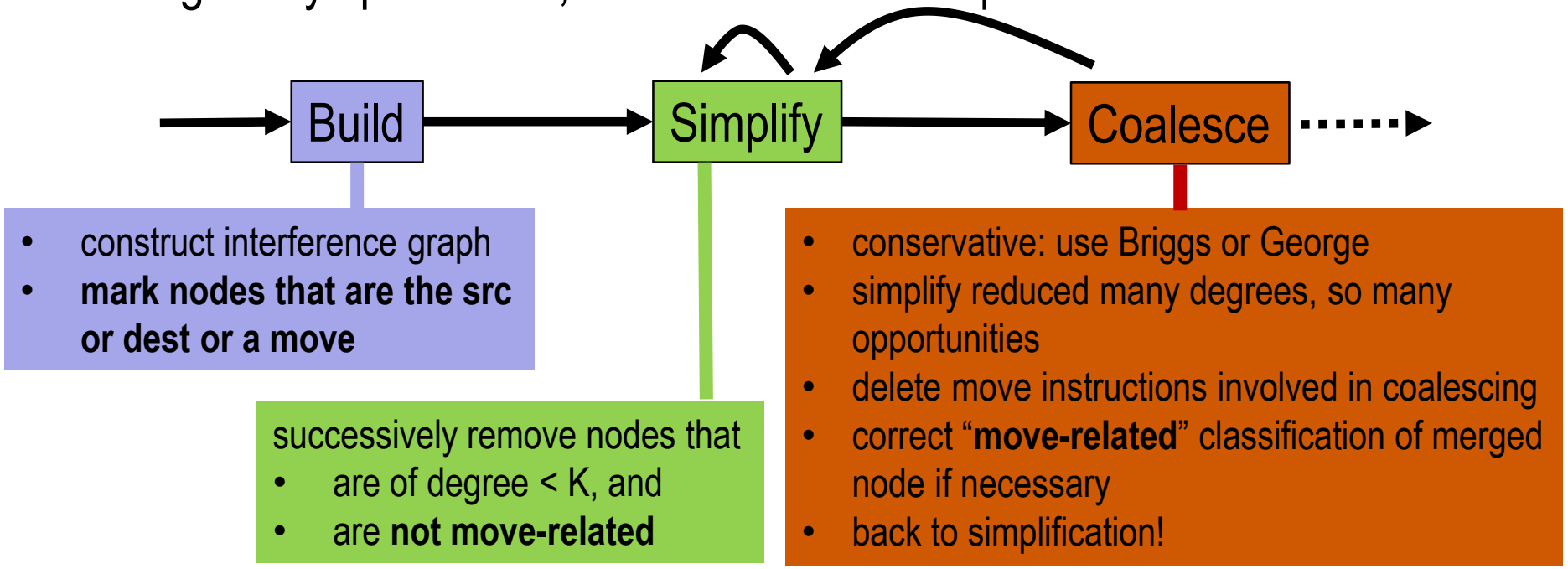
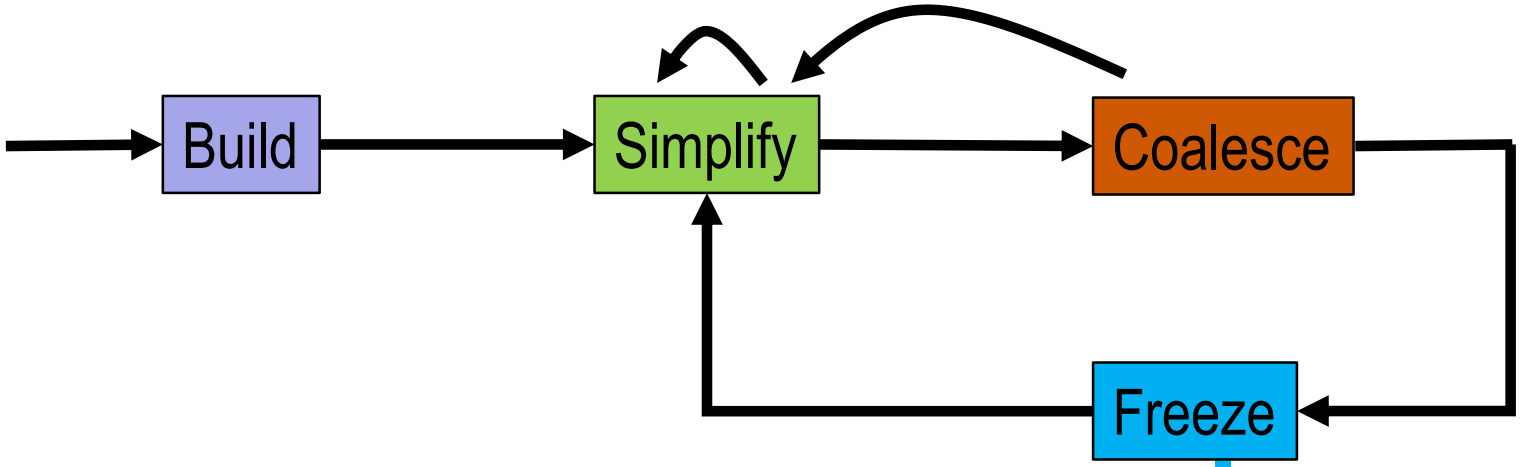


Allocation with coalescing: freezing

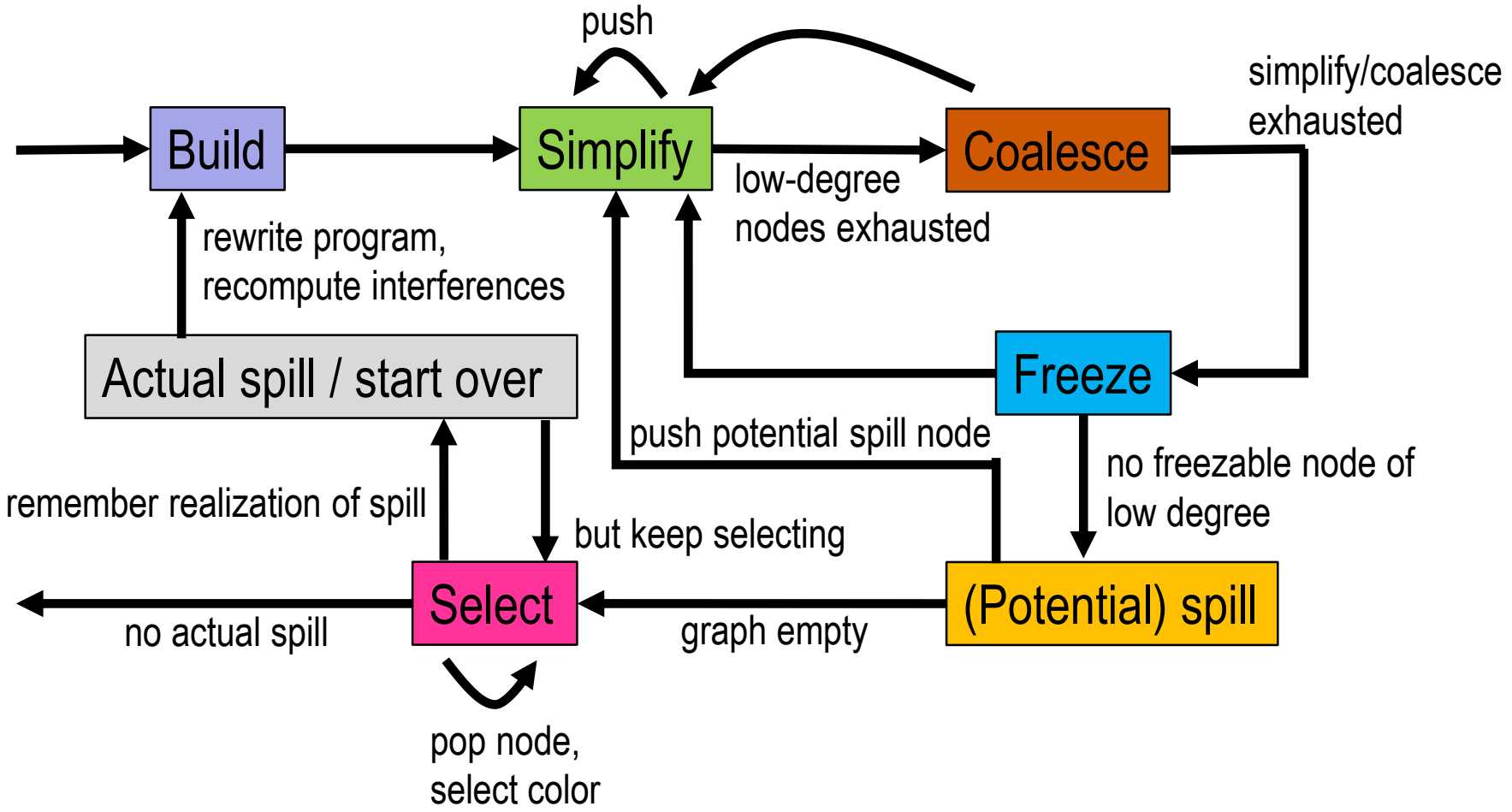


NEW PHASE:

- select a low-degree node **n** that is marked **move-related**
- mark it **non-move-related**
  - "give up hope to ever coalesce it"
  - also mark **n**'s move-partner **non-move-related**, unless it participates in some other move(s)
- back to simplify: at least the now unmarked nodes can be simplified

Allocation with coalescing: completing the algorithm

Remaining phases as before:



Coloring with coalescing: example (K = 4)

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// liveIn: k, j
g := M [ j+12 ]
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f = g * h
e := M [ j + 8 ]
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c := e + 8
d := c
k := m + 4
j := b
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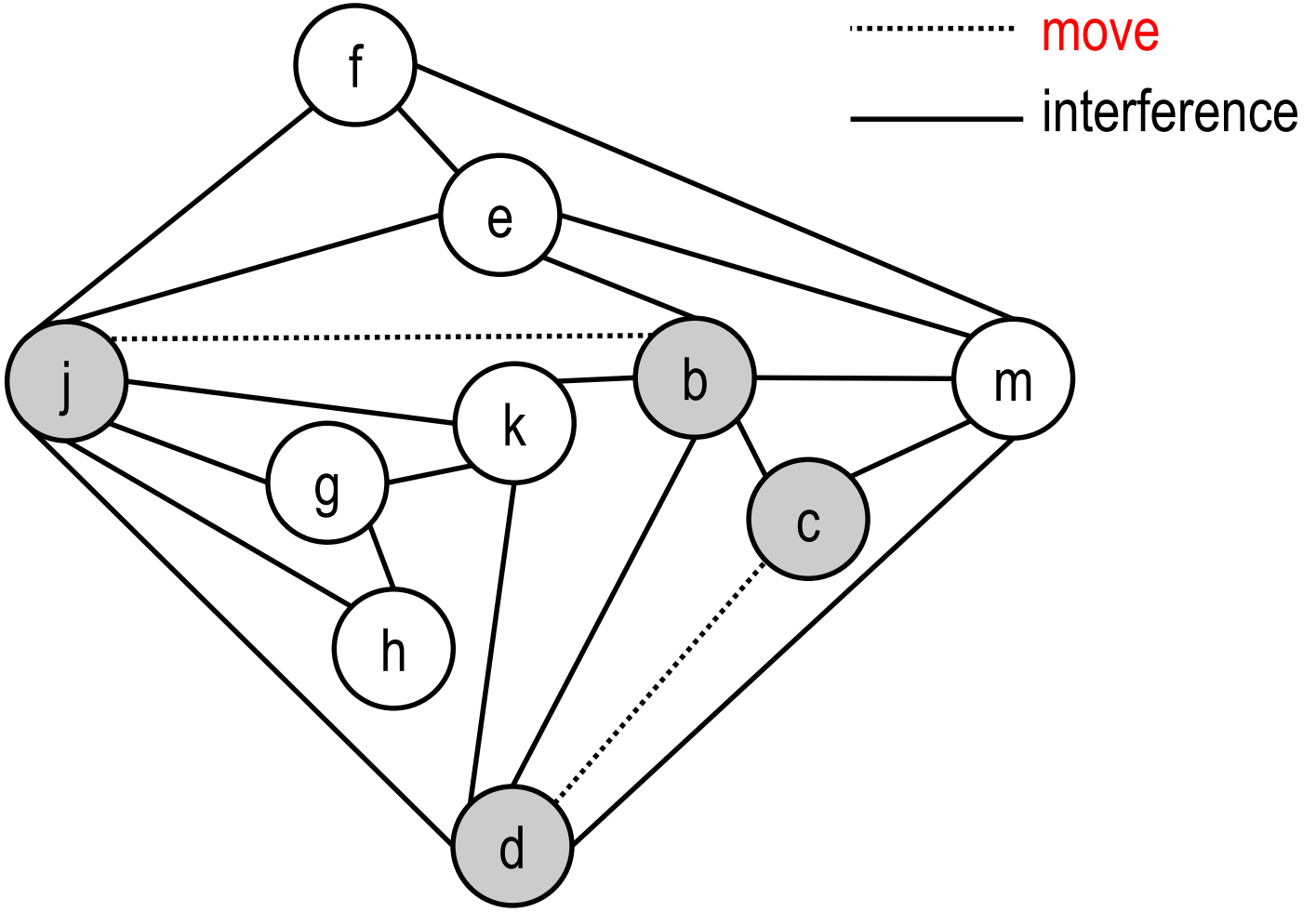

Non-marked nodes of degree < K: g, h, f

→ push g, h, k

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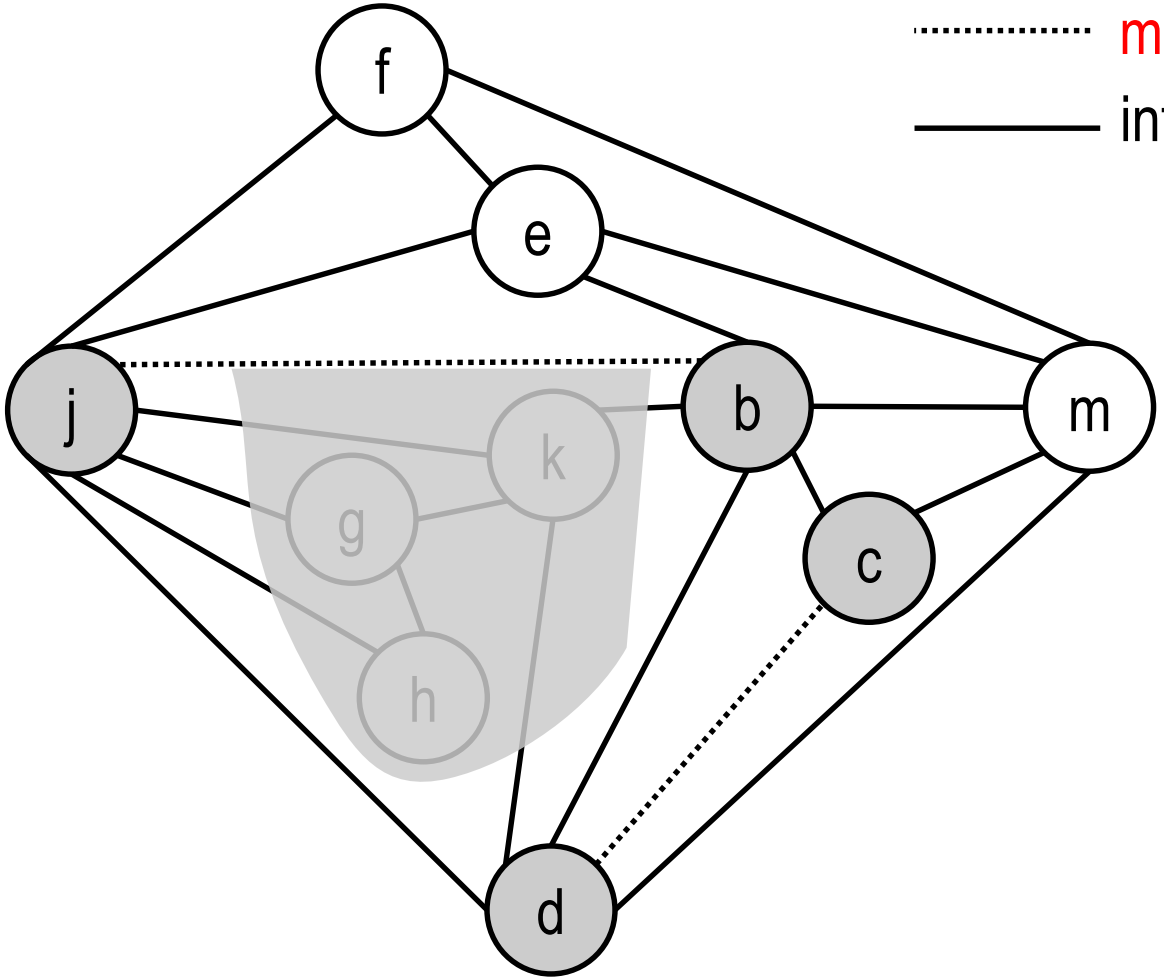

Non-marked nodes of degree < K: f

→ push g, h, k

could still simplify f instead!

Next: **coalesce** c & d

George: all neighbors of c already interfere with d

Briggs: merged node has < K neighbors of degree ≥ K

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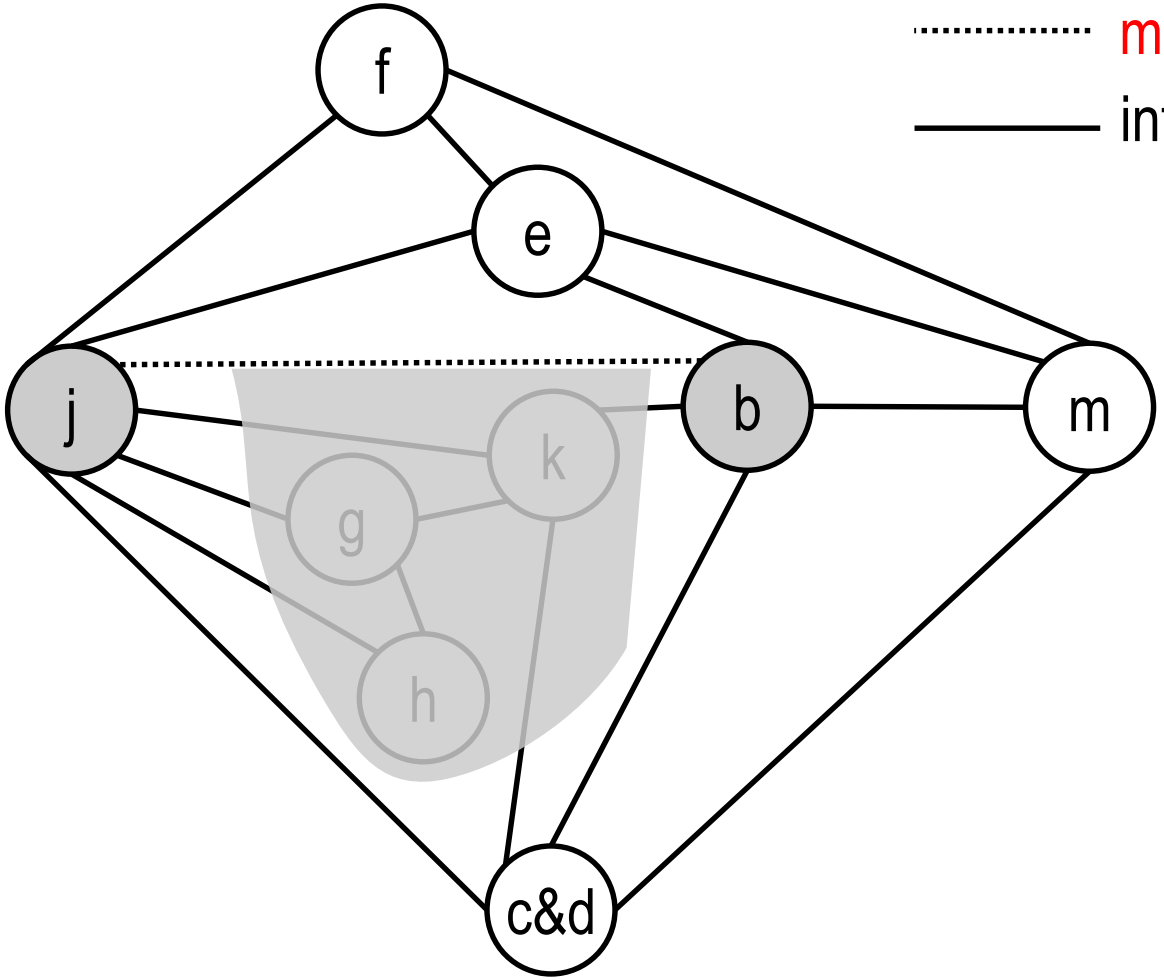

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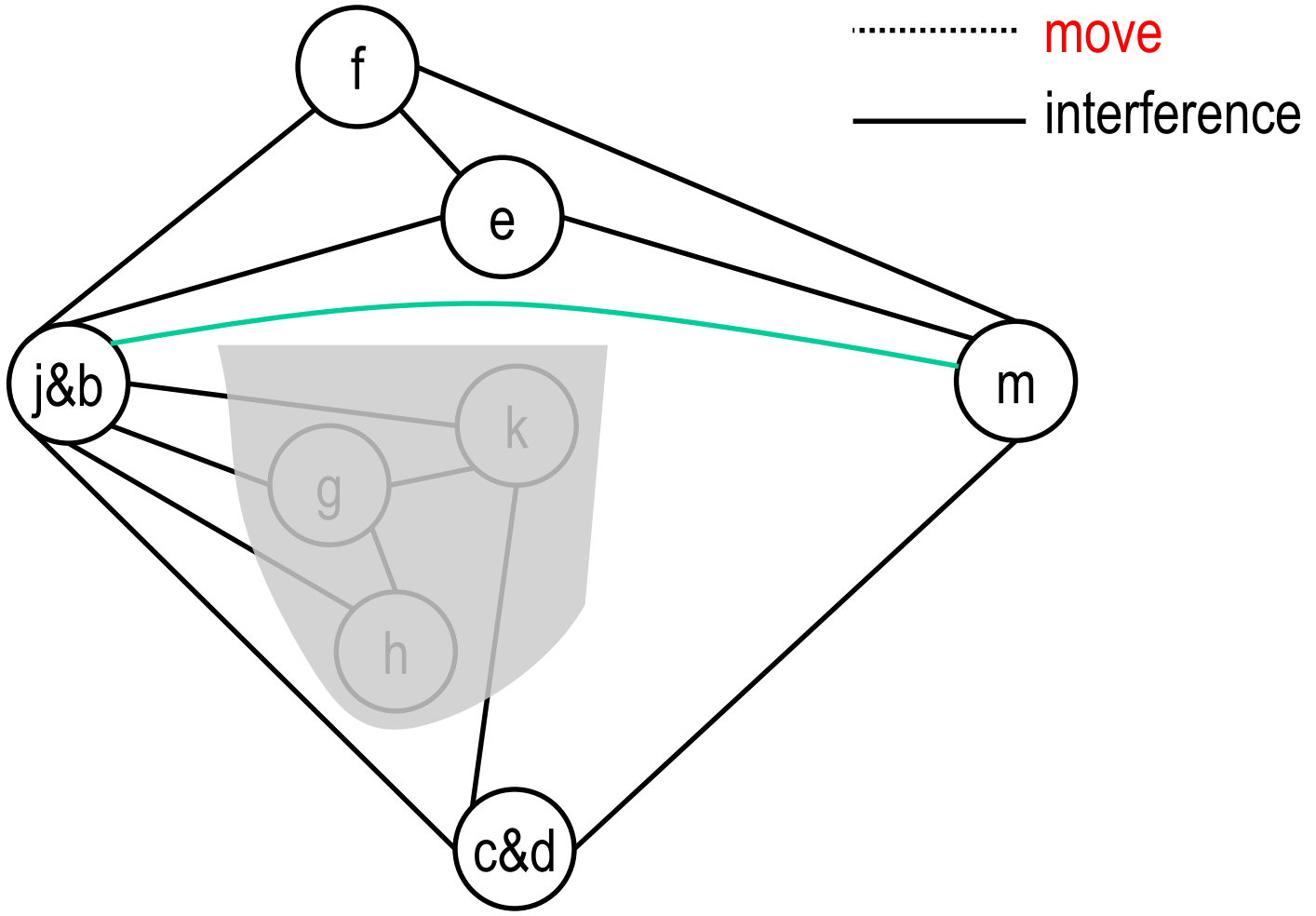

Non-marked nodes of degree < K: f, e, c&d

→ push g, h, k

Next: **push** c&d, j&b, f, m, e

pop e

Coloring with coalescing: example (K = 4)

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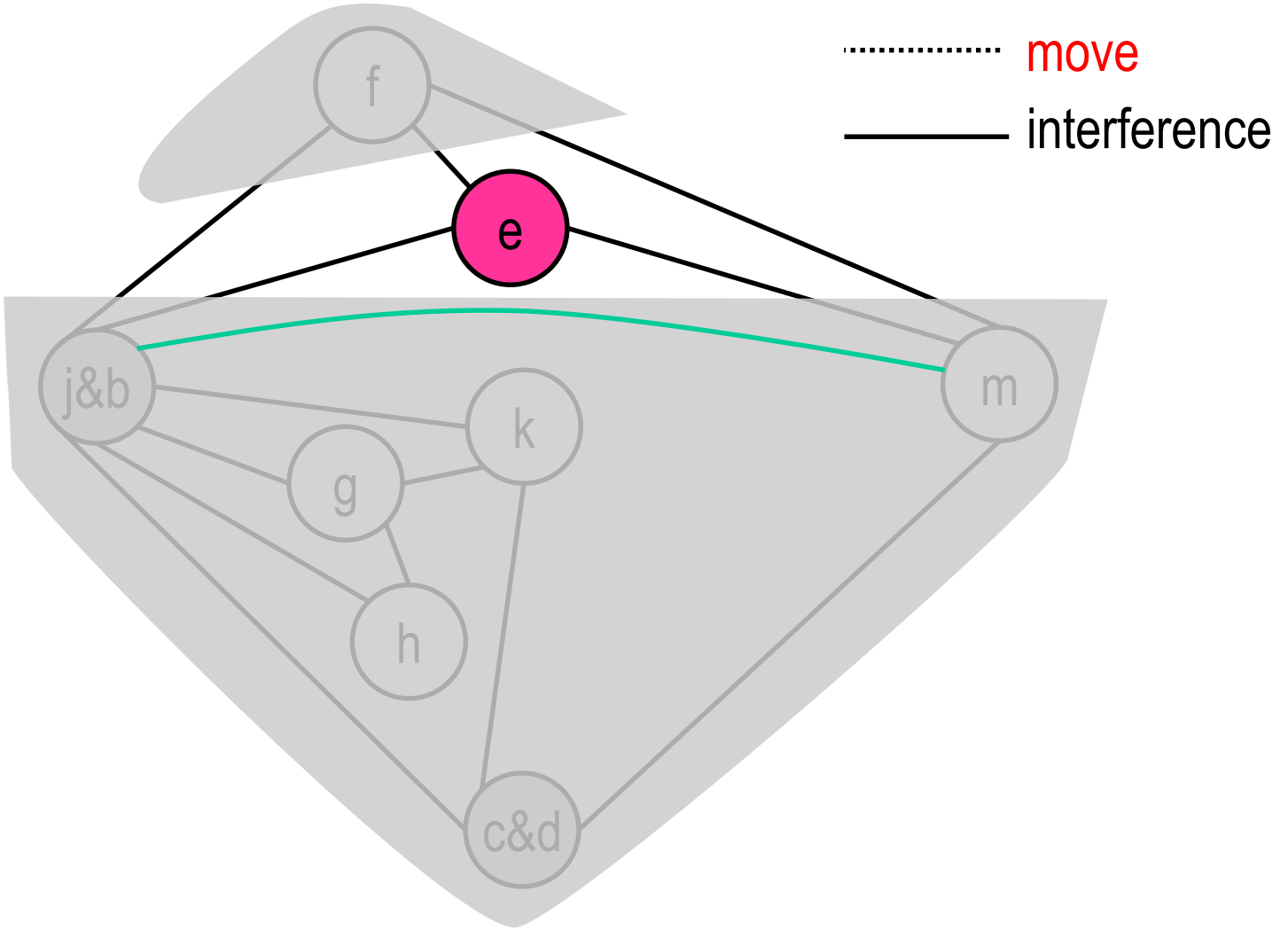

Non-marked nodes of degree < K:

→ push g, h, k, c&d, j&b, f, m

Next: **pop** m, f, j&b, c&d

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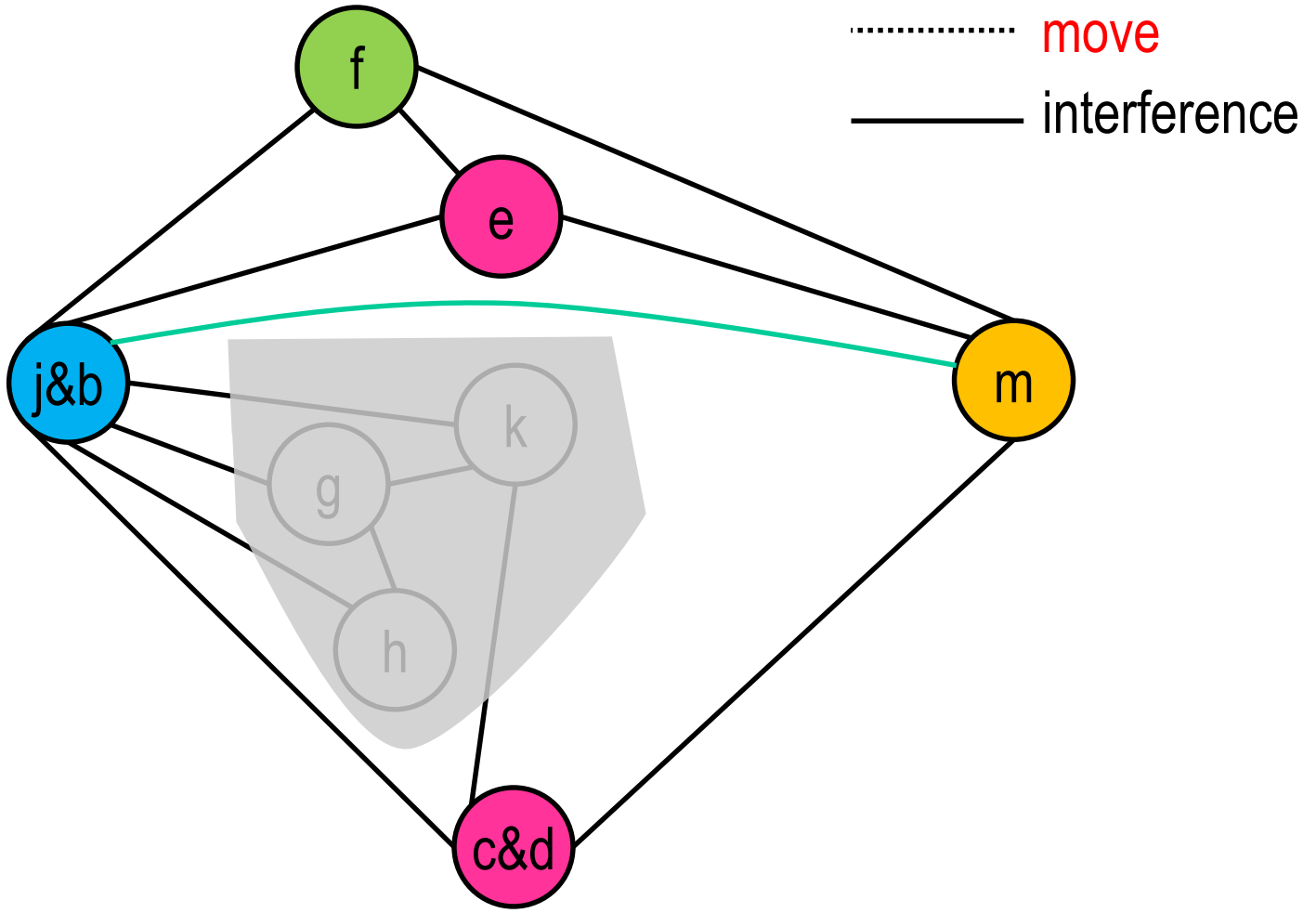

Non-marked nodes of degree < K:

→ push g, h, k

Next: **pop** k, h, g

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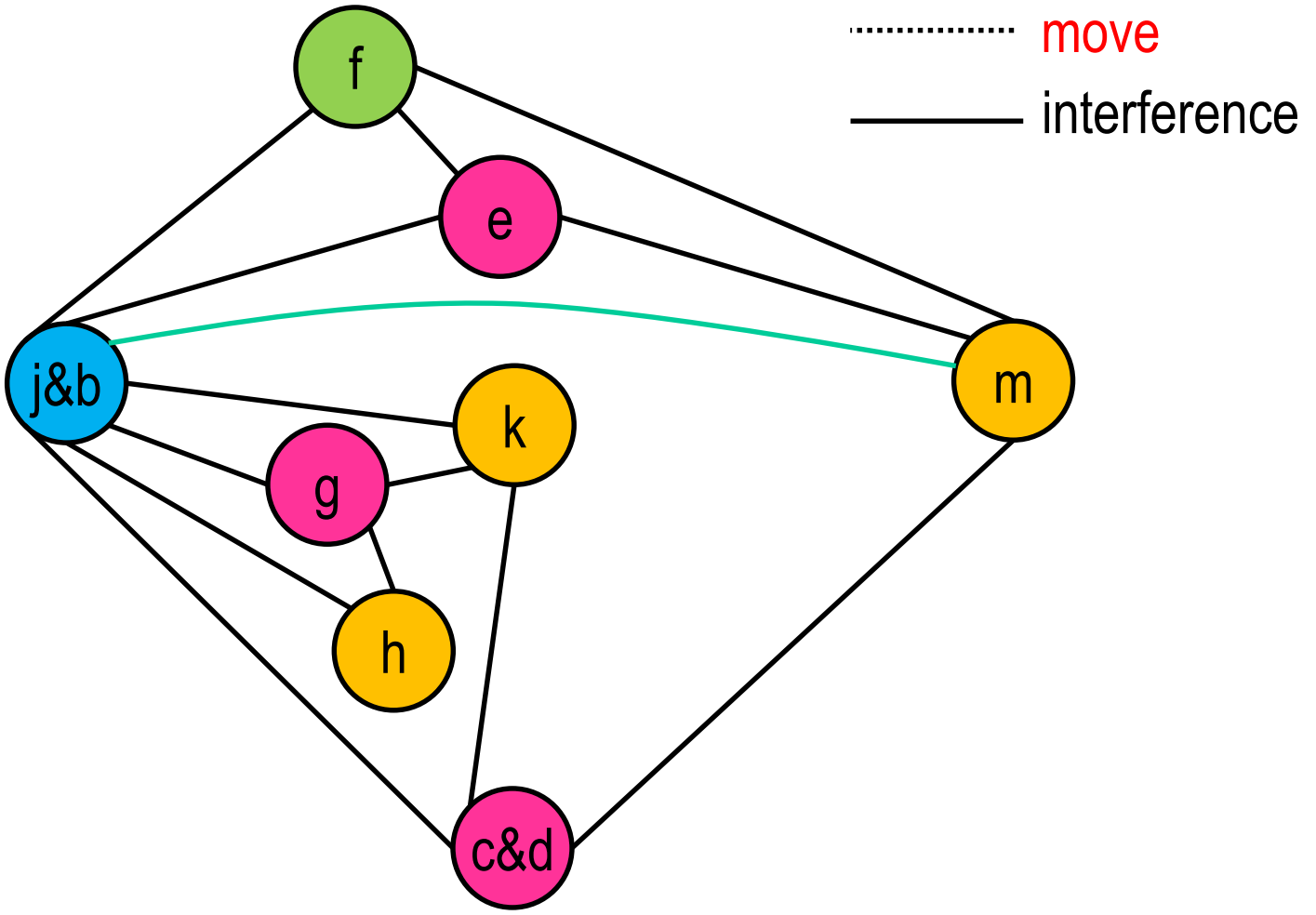

Done

Spilling heuristics

```
// liveIn: k, j
g := M [ j+12 ]
h := k – 1
f = g * h
e := M [ j + 8 ]
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M [ m_loc ] := m
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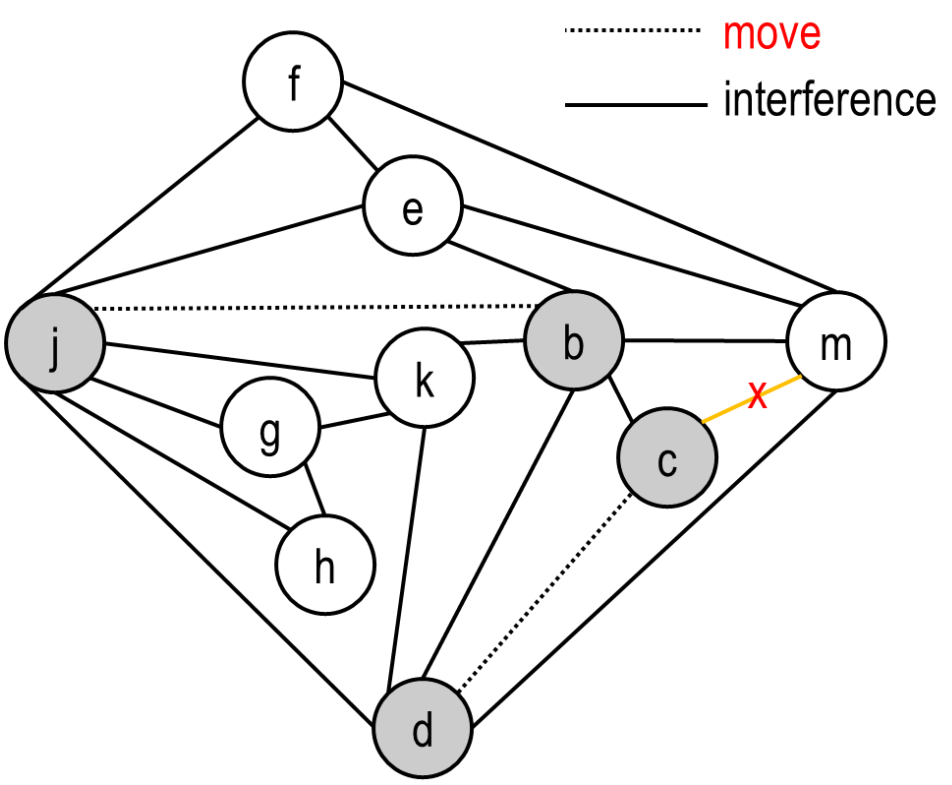

SPILL m

- splits single large liveness range of m into two short liveness ranges
- eliminates interference c ←→ m

General heuristics: spill nodes that

- have high degree, but few uses
- particularly if the live-range is long but sparse

Spilling heuristics

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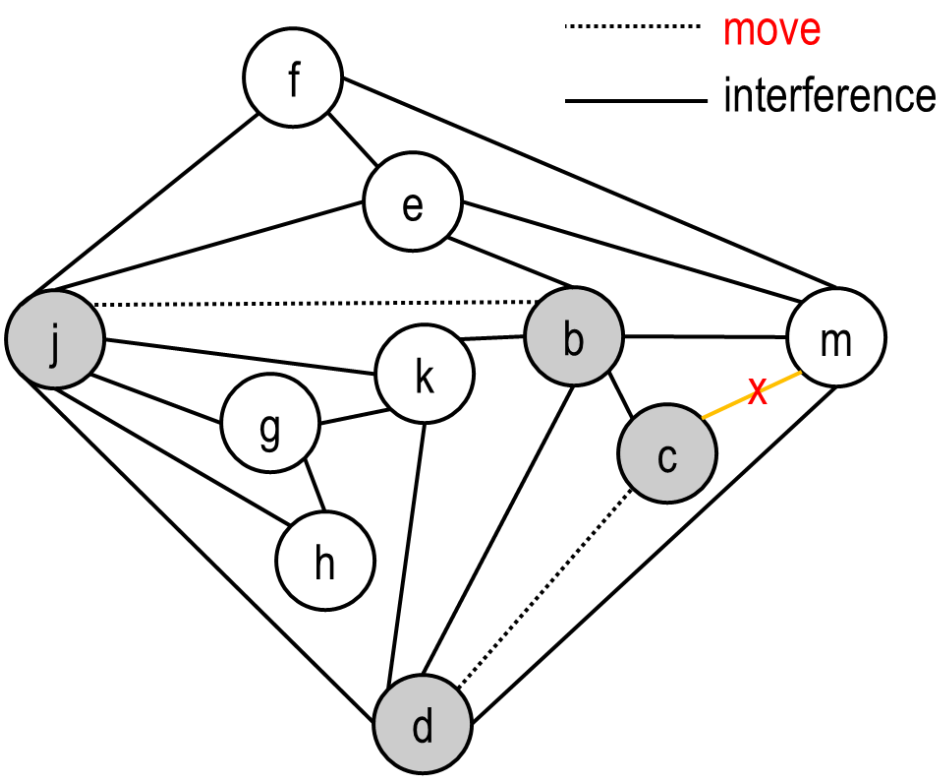

SPILL m

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Spilling heuristics

Naïve spilling: when rewriting program, undo all register coalescing
Improvement: remember all coalescing done before the first potential spill was discovered – they will tend to be rediscovered -- but undo the later coalescings.

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Coalescing spills:

- many spill locations → large stack frames
- don't need to keep spill locations apart if their virtual registers don't interfere!
- further benefit: eliminate spill-to-spill-moves:
  a ←b when both a and b are spilled:
  $t \leftarrow M[b_{loc}]; M[a_{loc}] \leftarrow t$ (typo in MCIL here – see errata list!)

Hence, can use coloring to minimize spill locations:

- infinitely many colors: no bound on size of frame
- liveness info yields interference between spilled nodes
- first, coalesce all spill nodes related by moves
- then, simplify and select (try to reuse colors)
- resulting # colors is # spill locations

All done during "Start Over", before spill code is generated and new register interference is computed

Precolored temporaries / nodes

- some temporaries correspond directly to machine registers: stack / frame pointer, standard argument registers 1 & 2, …
- these special temporaries implicitly interfere with each other
- but: ordinary temporaries **can** share color with precolored node (see example below)

Precolored temporaries / nodes

- some temporaries correspond directly to machine registers: stack / frame pointer, standard argument registers 1 & 2, …
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- but: ordinary temporaries **can** share color with precolored node (see example below)

K-register machine:

- introduce precolored K nodes, all interfering with each other
- liveness range of special-purpose registers (frame pointer etc) interfere with all ordinary temporaries that are live
- general-purpose registers have no additional interferences
- precolored nodes can't be simplified (they already have a color!), and can't be spilled (they are registers!)
- hence, consider them to be of infinite degree and start selection phase not from empty graph but graph of precolored nodes
- to keep live ranges of precolored nodes short, front-end can "copy them away", to freshly introduced temps

“Copying away” precolored temporaries

- suppose register r7 is callee-save:
  - considering function entry as definition of r7, and function exit as use ensures it’s live throughout the body, so it will be preserved
  - but: we don’t want to block the callee-save-register color for the entire body

```
entry: def(r7)
         :
exit: use(r7)
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  - so: introduce a new temporary t and insert moves
  - if register pressure is low, allocator will coalesce and eliminate moves
  - if register pressure is high, allocator will spill

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entry: def(r7)
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entry: def(r7)
       t ← r7
        :
       r7 ← t
exit: use(r7)
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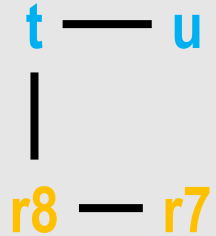
Note: the thus introduced temps t (one for each callee-save register) interfere with each other, with “later” other callee-save regs, and with most variables defined + used in the body, and are hence of “high degree and low #uses”.

```
entry: def(r7, r8)
       t ← r7
       u ← r8
        :
       r8 ← u
       r7 ← t
exit: use(r7, r8)
```



Liveness-across-call and caller/callee-save preference

```
Body of g():
    :
  x := 5
  y := x + 1
  z := f ()
  return z + y
```

Temporary x is not live across the call to f

- allocating x to a callee-save register r will force body of f to store r away to some t (previous slide), and restore r before returning
- but caller does not need x

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- but caller does not need **x**
- prefer allocation of **x** to caller-save register **s**:
  - callee f is free to overwrite **s**
  - that's ok: **x** is not used after function return
  - caller even does not even need to store **s** away prior to call – and knows this (liveness info)

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Temps not live across calls should be allocated to caller-save registers.

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- but caller does need y/s after function return
- so y/s would additionally need to be spilled / copied away prior to call
- we don't want to spill all variables that are live across calls!

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- prefer allocation of y to callee-save register r:
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  - no additional work needed on caller side

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Liveness-across-call and caller/callee-save preference

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How can we nudge the allocator to do this?

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In **CALL** instruction, understand all **N caller-save registers** to be defined/live-out. They interfere with **each other**

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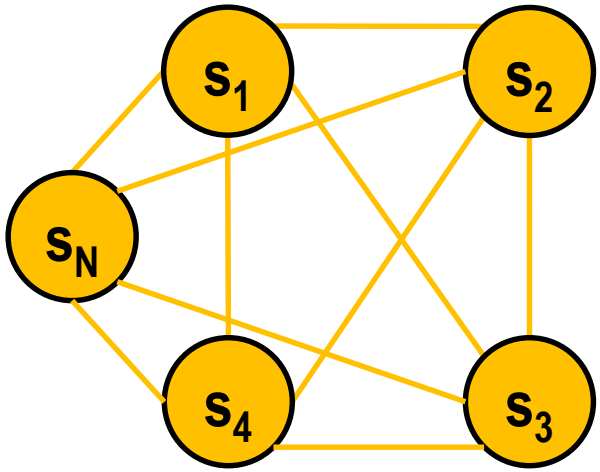

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How can we nudge the allocator to do this?

In **CALL** instruction, understand all **N caller-save registers** to be defined/live-out. They interfere with **each other but not with x**, so a good allocator will tend to assign **x** to the precolor of one of the s_i.

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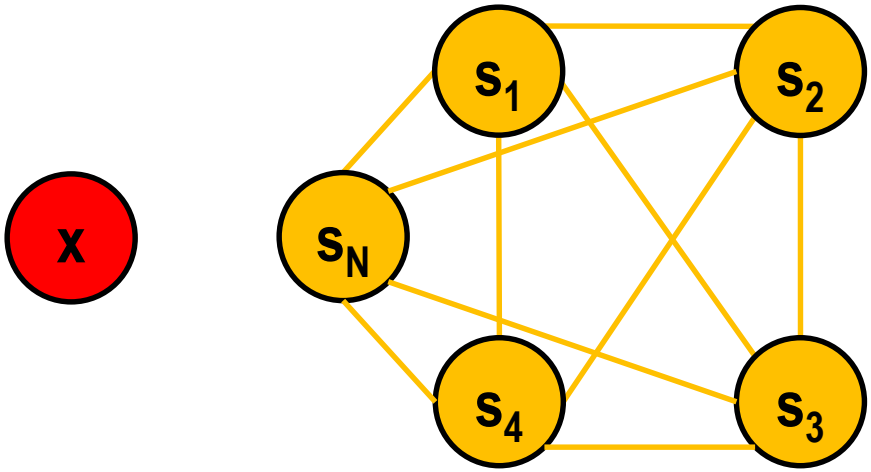

Liveness-across-call and caller/callee-save preference

Temps live across calls should be allocated to callee-save registers.

How can we nudge the allocator to do this?

In **CALL** instruction, understand all **N caller-save registers** to be defined/live-out. They interfere with **each other and also with y.**

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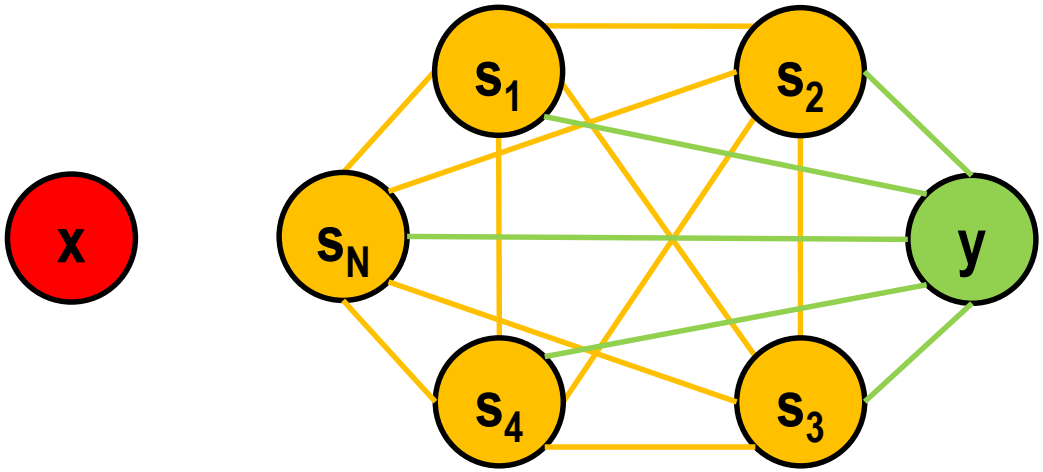

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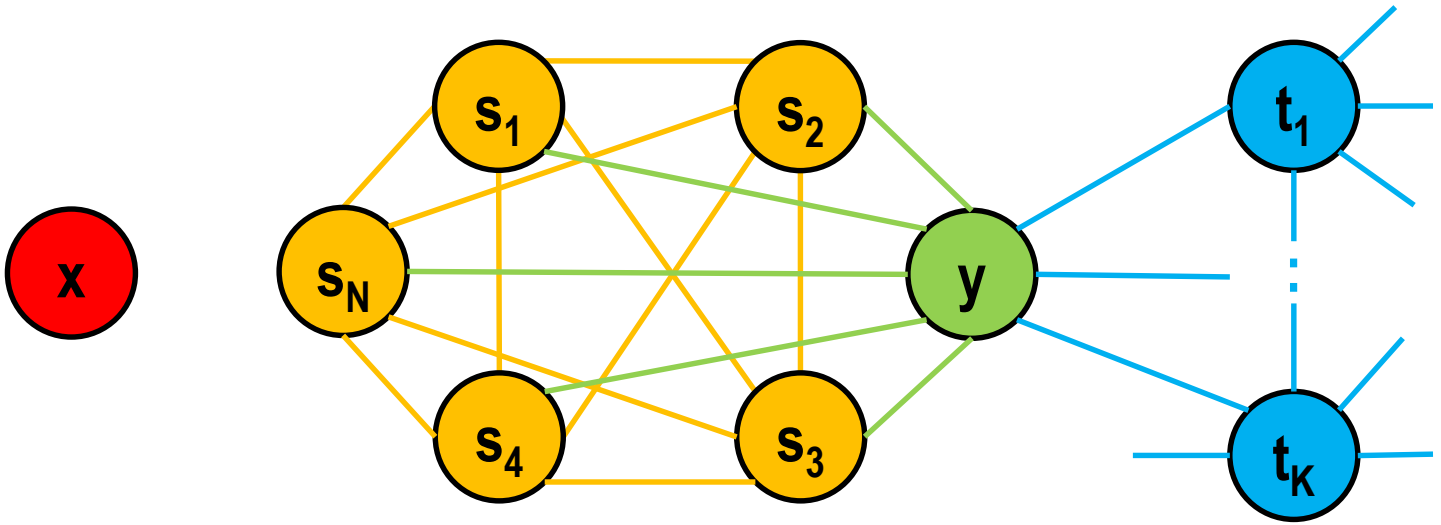

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Temps live across calls should be allocated to callee-save registers.

How can we nudge the allocator to do this?

In **CALL** instruction, understand all **N caller-save registers** to be defined/live-out. They interfere with **each other and also with y.** But **y** also interferes with the t_i created by the front-end in the body of g. So a spill is likely. Since the t_i are "high degree, **low use**", they are more likely to be selected for spill. So, the color of one callee-save registers is available for **y**.

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Body of g():
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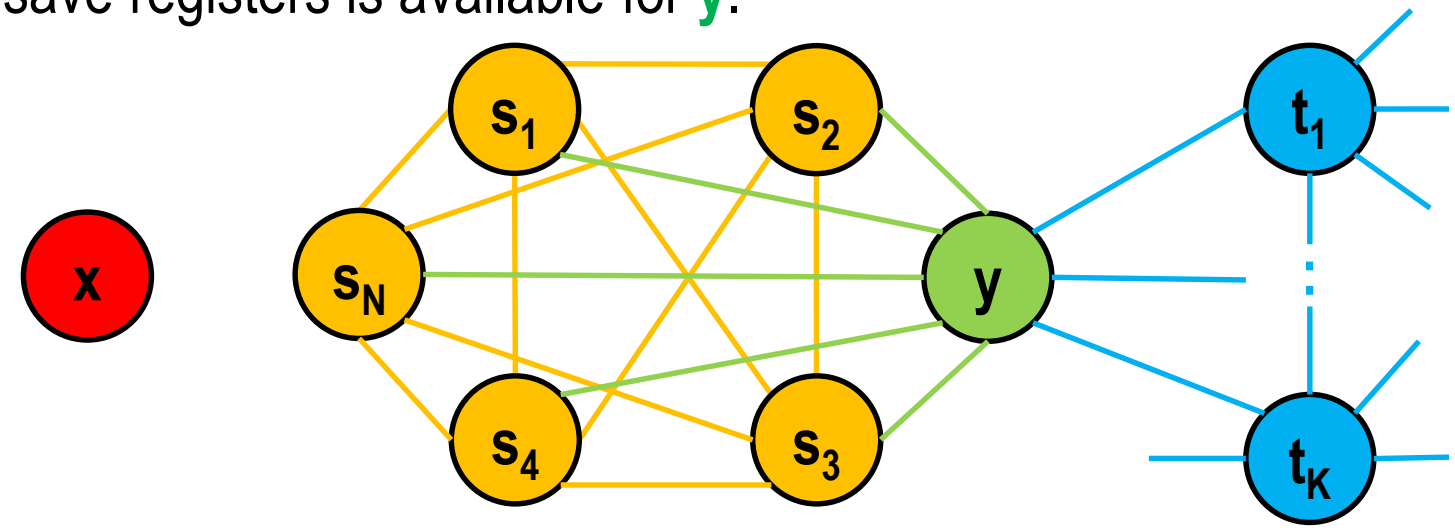
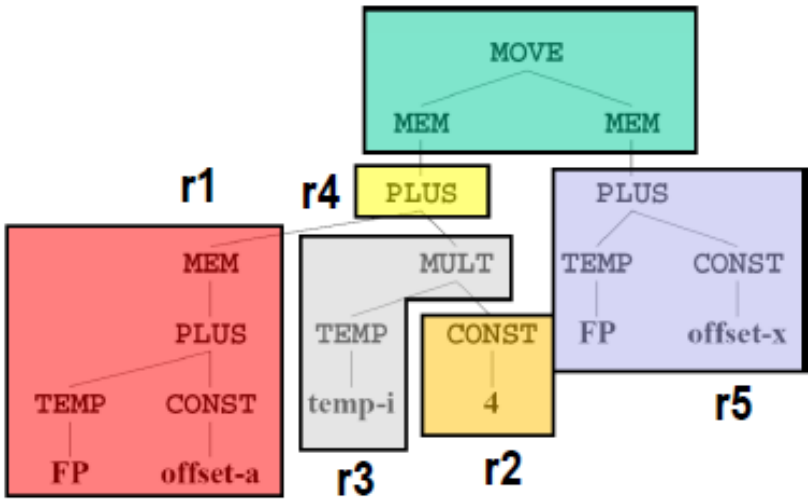


Register allocation for expression trees

Can avoid liveness calculation, interference graph construction, coloring.

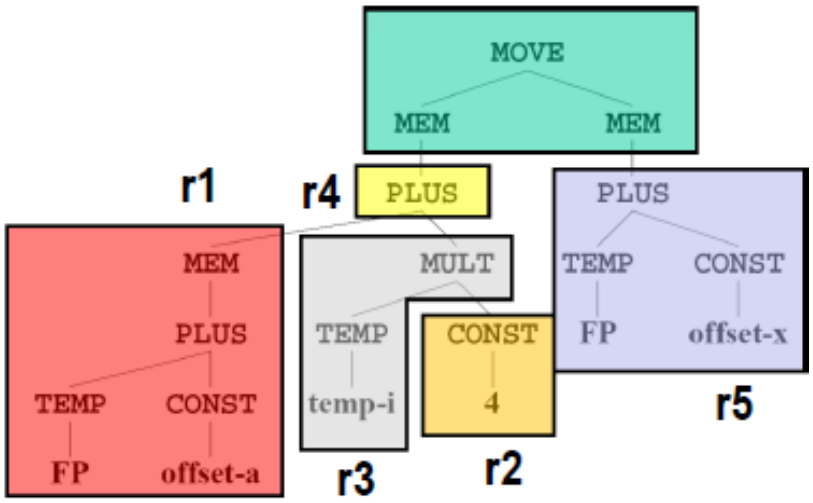
Flashback to instruction selection: “tiling”, ie covering the tree with patterns corresponding to machine instructions.



In IR phase, had suggested use of separate (virtual) registers for each tile.

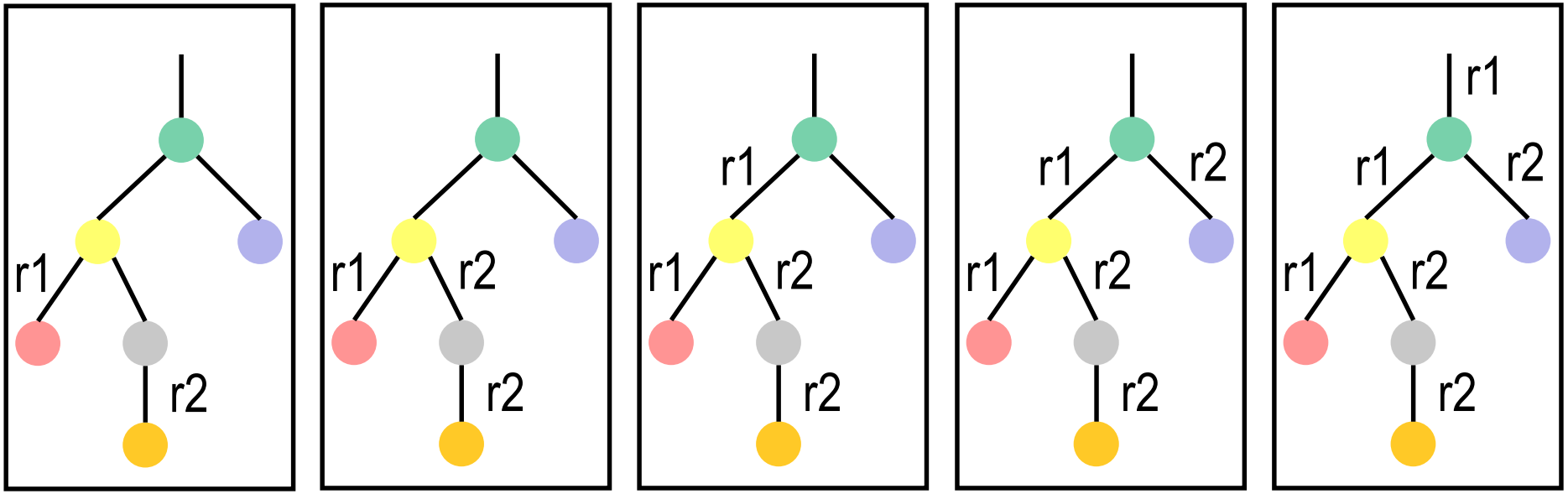
Clearly, can do better…

Register allocation for expression trees



Algorithm 1:

- simple postorder traversal
- can be combined with maximal munch (optimal but not optimum)



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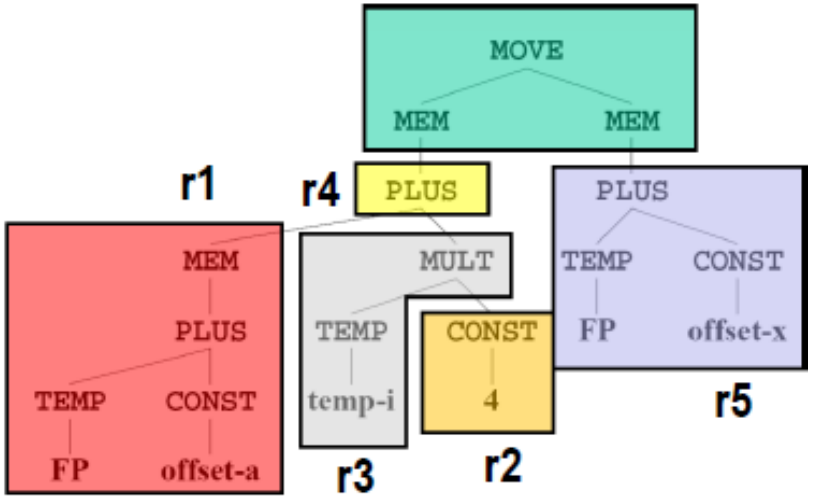

Algorithm 2:

- dynamic programming
- label each tile with number of registers needed for its evaluation
- when visiting node u with children u_{left} u_{right}, with needs n_l and n_r, respectively:
  - evaluating left child; hold result while evaluating right child: cost = $\max(u_{left}, 1 + u_{right})$
  - evaluating right child; hold result while evaluating left child: cost = $\max(1 + u_{left}, u_{right})$
  - choose cheaper evaluation order