COS/ELE 375 Assignment 2

Fall 2015, Princeton University

Due date: 10/22/15

Submission guidelines:

Your course enrollment (COS/ELE 375) and date of submission should be listed with your name on the front page of your submission. Please submit your assignment in class or in the box outside of CS-241.
LATE SUBMISSIONS: Record the date and time of your submission.

Problems:

1. What is the worst case delay of a 1-level 5-bit carry look ahead adder and ripple-carry adder (in terms of # of gate delays)? Which set of input combinations cause the worst case delay? Elaborate with reasons.

2. Design a 6-bit Shifter (left & right logical and arithmetic) which allows a maximum shift of 4-bits. You need not implement any other instructions.

3. Prove that a sign extension of any length correctly maintains the value of all 2's complement numbers.

4. Why is the 2's complement representation used most often? Give an example of overflow when:

   - 2 positive numbers are added
   - 2 negative numbers are added
   - A-B where B is a negative number

5. Consider the following idea: Let's modify the instruction set architecture and remove the ability to specify an offset for memory access instructions. Specifically, all load-store instructions with nonzero offsets would become pseudoinstructions and would be implemented using two instructions. For example:

   ```
   addi $at, $t1, 104 # add the offset to a temporary
   lw $t0, $at # new way of doing lw $t0, 104($t1)
   ```

   What changes would you make to the single-cycle datapath and control if this simplified architecture were to be used? Feel free to use the figure on the next page.

6. Consider a change to the multiple-cycle implementation presented in lecture that alters the register file so that it has only one read port. Neatly describe (via a diagram) any additional changes that will need to be made to the datapath in order to support this modification. Describe (via another diagram) the changes to the finite state machine necessary to make the instructions (LW, SW, R-type, BEQ, J) work with your new datapath.

PCSrc

Add
ALU result

Shift left 2

MemtoReg
M u x 1 / 0

Read data
Data memory
MemRead

MemWrite
Address
Write data

Zero
ALU result
ALU

ALUSrc
M u x 1 / 0

ALU control
ALUOp

RegWrite

Read register 1
Read register 2
Write register
Write data
Registers

Read data 1
Read data 2

Sign extend
32
16

Instruction [5–0]

Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]

M u x 1 / 0
RegDst

Add
4

PC
Read address
Instruction [31–0]
Instruction memory