ELE 375 Final Exam
Fall, 2000
Prof. Martonosi

Question	Score
1	/10
2	/20
3	/15
4	/15
5	/10
6	/20
7	/20
8	/25
9	/30
10	/30
11	/30
12	/15
13	/10
Total	**/ 250**

Please write your answers clearly in the space provided. For full credit and/or to get partial credit, show your work.

Name: _____

Honor code:

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1. (10 points) The first level of the cache hierarchy usually involves separate level-one instruction and data caches. Give two good reasons for keeping the caches split (separate) at this level of the hierarchy.

2. (20 points) The design team for a simple, single-issue processor is choosing between a pipelined or non-pipelined implementation. Here are some design parameters for the two possibilities:

Parameter	Pipelined Version	Non-Pipelined Version
Clock Rate	50MHz	30 MHz
CPI for ALU instructions	1	1
CPI for Control instructions	2	1
CPI for Memory instructions	2	1

   a. (10 points) For a program with 30% ALU instructions, 10% control instructions and 60% memory instructions, which design will be faster and why?

   b. (10 points) For a program with 60% ALU instructions, 10% control instructions and 30% memory instructions, which design will be faster and why?

3. (10 points) As lead designer on a CPU design team, you have the choice of devoting hardware either to an additional floating-point unit or to a larger cache. If you do not include the additional FP unit, the penalty will be 10 additional cycles on the 10% of instructions that are affected in your workload. On the other hand, if you do not include the enlarged cache, the penalty will be 1 additional cycle on the 30% of instructions that are affected in your workload. Starting from a base CPI of 1, which would you choose to implement and why? Use the CPU performance equation to justify your choice.

4. (15 points) For each of the characteristics below, complete the table by checking the appropriate entry (architecture or implementation) to indicate whether each feature is most often a characteristic of a computer architecture or of a particular CPU implementation.

Characteristic	Architecture?	Implementation?
# of bits in an instruction		
size of instruction cache		
# of registers visible to programmers		
miss penalty for L1 data cache		
Number of floating-point divider units		
RISC vs. CISC		

5. (10 points) Typically, instructions in the VAX instruction set have 3 source operands and 1 destination operand. If you aim to avoid structural hazards in a pipelined, single-issue VAX implementation, what is the minimum number of register file read and write ports that would be required?

6. (20 points) Amdahl's Law
   a. (10 points) Consider a workload where 50% of the execution time consists of multimedia processing for which the MMX instruction set extensions might be helpful. According to Amdahl's law, what is the maximum speedup that can be achieved by implementing them?

   b. (10 points) Now say that you work at Intel and MMX designers claim that multimedia code sequences will see a 3.5X speedup by using MMX extensions. What fraction of the original execution time must be multimedia code in order to achieve an overall speedup of 1.8X?

7. (25 points) How many total SRAM bits will be required to implement a 64KB direct-mapped, physically-indexed cache with 32 byte lines and a single valid bit per entry? Assume that the physical address is 50 bits wide.

8. (30 points) Consider a 128 byte, direct-mapped cache with 16 byte lines. A data reference stream is presented to the cache in the order shown below. (Each reference is a read of a single 32-bit word starting at the given address.) For each reference, indicate whether it is a hit or a miss. Compute the miss rate and write it in the space provided.

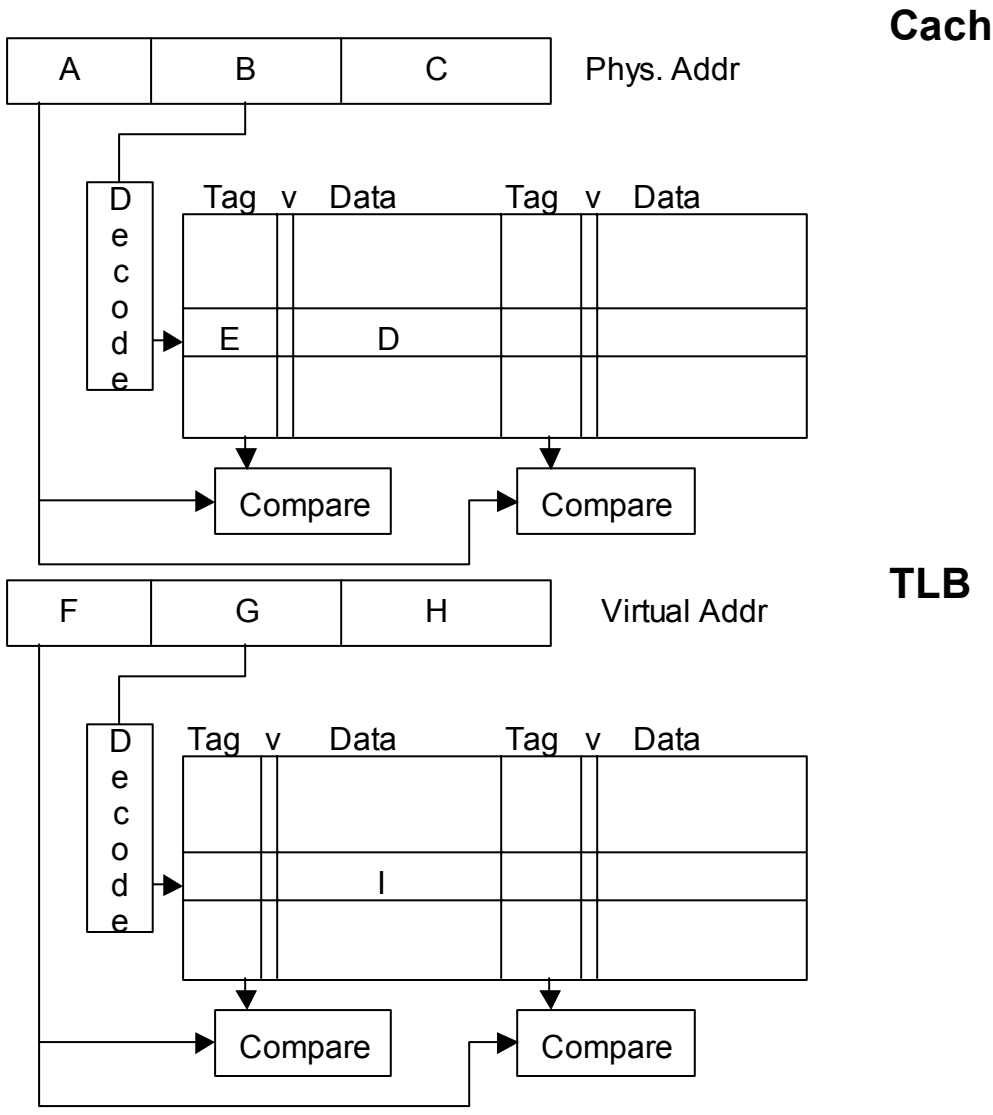
Address Referenced	Hit or Miss?
36	
32	
190	
36	
40	
194	
198	
48	
52	
318	
32	
56	
194	
198	
202	

9. (25 points) Consider a memory system with the following parameters:

- Translation Lookaside Buffer has 256 total entries and is 2-way set associative
- 64Kbyte L1 Data Cache has 64 byte lines and is also 2-way set associative
- Virtual addresses are 32-bits and physical addresses are 24 bits
- 8KB page size

The figures below are labeled diagrams of the cache and TLB. Please fill in the appropriate information in the boxes below:

L1 Cache		TLB	
A =	bits	F =	bits
B =	bits	G =	bits
C =	bits	H =	bits
D =	bits	I =	bits
E =	bits		



10. (30 points) Pipelining
    a. (15 points) First consider a standard 5-stage pipeline of the type discussed in class: IF-ID-EX-M-WB. The only difference is that the pipeline here implements **NO BYPASSING**. All data dependences are handled by having the pipeline stall until the register fetch will result in the correct data being fetched. For the following pairs of instructions, indicate the number of stall cycles required between **instruction i** and **instruction i+1**:

Instruction i	Instruction I+1	# Stall cycles
add r1, r2, r3	add r4, r1, r5	
add r1, r2, r3	sw r1, 42(r8)	
lw r1, 10(r7	add r11, r1, r9	

    b. (15 points) Next consider a non-standard 6-stage pipeline as described below. Once again, the pipeline implements NO BYPASSING as in part (a). Please again complete the stall cycles for each of the cases given.

IF Instruction Fetch
ID Instruction Decode
RF Register fetch during second half of cycle
EX ALU execution, memory address calculation
M Memory operation
WB Writeback to register file during first half of cycle

Instruction i	Instruction I+1	# Stall cycles
add r1, r2, r3	add r4, r1, r5	
add r1, r2, r3	sw r1, 42(r8)	
lw r1, 10(r7	add r11, r1, r9	

11. (25 points) A program repeatedly performances a three-step process: It reads in an 8-KB block of data from disk, processes that data, and then writes out the result as another 8KB block elsewhere on the disk. Each block is contiguous and randomly located on a single track on the disk. The disk drive rotates at 7200 RPM, has an average seek time of 12 ms, and has a transfer rate of 20 MB/sec. The controller overhead is 5 ms. No other program is using the disk or processor. The processing step takes 20 million clock cycles each time and the clock rate is 400 MHz.

    a. (15 points) First, assume there is no overlapping of disk operation with processing. What is the overall speed of the system in blocks processed per second?

    b. (10 points) Discuss a scheme for achieving maximal overlap of disk and processing and compute what the overall speed (blocks processed per second) would be with your scheme.

12. (15 points) I/O Bandwidth: You are visiting your Uncle Ebeneezer who lives in Lawrenceville, NJ. You have a choice of how to get him a 40Mbyte document he wants from the internet. Compute the bandwidth (megabytes per second) of both options and discuss which is the better option.

    a. Option 1: Download the document via your uncle's 9600 baud (bits per second) modem, which he bought in 1988 for $500. Assume that the modem speed is the only factor which affects your download time (eg no internet congestion elsewhere, etc.)

    b. Option 2: Drive from Ebeneezer's house to campus, download the document at 10Mbyte per second, and then drive back to Ebeneezer's house. Assume that the drive to campus (including starting, stopping, parking, etc.) takes 15 minutes each way.

    c. What is the document size at which these two options take the same amount of time?

13. (10 points) DRAM
    a. (5 points) Which will require more transistors? A 32Kbit x 1 SRAM or a 64Kbit x 1 DRAM

    b. (5 points) How many address pins are needed for a 256Kbit x 1 DRAM?